ACER_BAP31

MAIN BOARD

2008.12.29

DATE	CHANGE NO.	REV
Tuesday, March 10, 2009		X01

	EE	DATE	POWER	DATE
DRAWER				
DESIGN				
CHECK				
RESPONSIBLE				

SIZE= VER:
FILE NAME: XXXX-XXXXXX-XX
P/N XXXXXXXXXXXX

INVENTEC

TITLE ACER_JM31

SIZE	CODE	DOC.NUMBER	REV
C	X01	D-CS-1310A2264501-ALG	X01

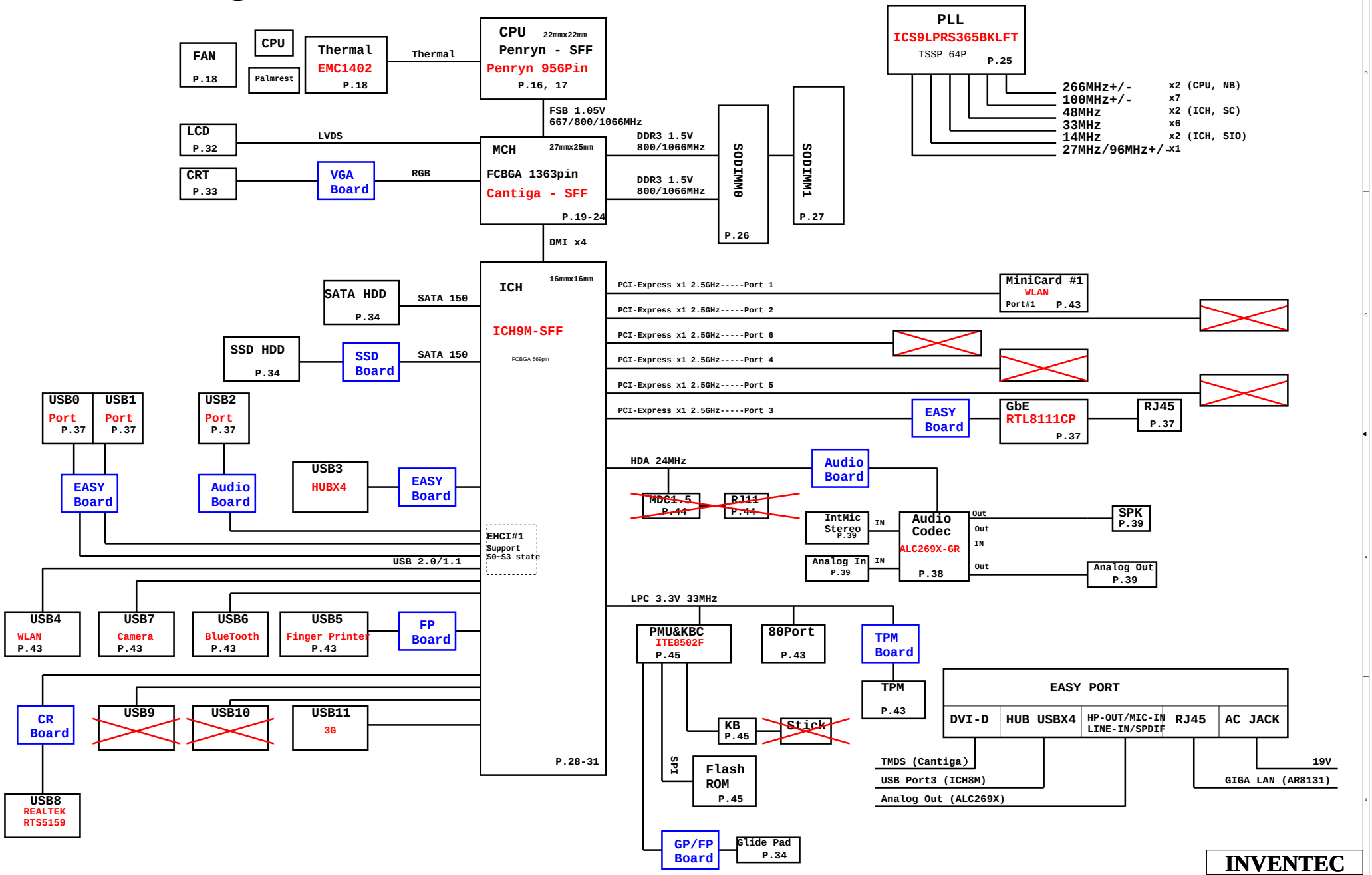
SHEET 1 of 36

1. Schematic Page Description :

Montevina Schematic Ver : X01

1. Title
2. Schematic Page DESCR
3. Block Diagram
4. Annotations
5. Schematic Modify
6. Timing Diagram
7. Power Block Diagram
8. Adaptor in/Charge
9. 5VLA/5VA/3VA
10. 3VS/5VS/1.5V (DDR3)
11. 1.05VS/1.5S/1.8V/1.5VA
12. Power Latch/1.5VS/SCREW HOLE
13. CPU Core Power
14. GPU Core Power
15. Penryn Processor(1/2)
16. Penryn Processor(2/2)
17. CPU Thermal
18. Cantiga Host(1/6)
19. Cantiga DMI/Graph(2/6)
20. Cantiga DDRII(3/6)
21. Cantiga Power(4/6)
22. Cantiga Power(5/6)
23. Cantiga Ground(6/6)
24. Clock Generator
25. DDR3 SDRAM SO-DIMM0
26. DDR3 SDRAM SO-DIMM1
27. ICH9M CPU/IDE/SATA(1/4)
28. ICH9M PCI/PCIE/DMI/USB(2/4)
29. ICH9M GPIO(3/4)
30. ICH9M Power/GND(4/4)
31. LCD CNN/SATA/3G/WLAN
32. KBC ITE8512F
33. IO CN

3. Block Diagram :



INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET

CHANGE by Miles Liu DATE Tuesday, March 10, 2009

4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

= Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM:	1.3319V~1.4375V~1.4591V	18A
	LFM:	0.9221V~0.9625V~0.9739V	
1.05VS	Penryn SFF : AGTL+ termination	1V~1.05V~1.10V	4.5A
	Cantiga GS: Core	0.997V~1.05V~1.102V	8.7A
	Cantiga GS: PCIE	0.9975V~1.05V~1.1025V	1.78A
	Cantiga GS:Core+IMEL+HSIO	0.9975V~1.05V~1.1025V	2.898A
	Cantiga GS:VCC_GMCH	0.997V~1.05V~1.102V	10.154A
	Cantiga GS:VCCA_SM_CK and NCTF	0.997V~1.05V~1.102V	37.95mA
	Cantiga GS:VCC_DMI	0.997V~1.05V~1.102V	456mA
	Cantiga GS:VCCA_SM	0.997V~1.05V~1.102V	747.5mA
	Cantiga GS:VTT	0.997V~1.05V~1.102V	852mA
	ICH9M:VCC1_05	0.997V~1.05V~1.102V	1.634A
	ICH9M:DMI	0.997V~1.05V~1.102V	48mA
	ICH9M:CPU_IO	0.997V~1.05V~1.102V	2mA
1.5VS	Penryn SFF PLL	1.425V~1.5V~1.575V	130mA
	Cantiga GS: QDAC	1.425V~1.5V~1.575V	0.5mA
	Cantiga GS: LVDS	1.71V~1.8V~1.89V	60.31mA
	Cantiga GS: TVDAC	1.425V~1.5V~1.575V	35mA
	Cantiga GS: Various PLLS analog supply	1.425V~1.5V~1.575V	485mA
	Cantiga GS: VCC_SM_CK	1.425V~1.5V~1.575V	149.5mA
	Cantiga GS: VCC_SM	1.425V~1.5V~1.575V	3.1625A
	ICH9M:PCIE_ICH	1.425V~1.5V~1.575V	646mA
	ICH9M:SATA_ICH	1.425V~1.5V~1.575V	1.342A
	ICH9M:VCC_GLAN	1.425V~1.5V~1.575V	80mA
	Mini Card:		
	Express Card:	1.425V~1.5V~1.575V	650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GS: HV CMOS	3.135V~3.3V~3.465V	105.3mA
	Cantiga GS: VCCS_TVDAC	3.135V~3.3V~3.465V	78mA
	ICH9M:VCC3_3	3.135V~3.3V~3.465V	308mA
	ICH9M:VCCGLAN3_3	3.135V~3.3V~3.465V	1mA
	Thermal Sensor:	3.0V~3.3V~3.6V	5mA
	Mini Card: UMTS		
	Express Card:	3.135V~3.3V~3.465V	1.3A
	CLK Generator: ICS9LPRS365BKLFT	3.135V~3.3V~3.465V	500mA
	Mini Card: WirelessLan		
	Bluetooth:		
	Super I/O: IT8305E	3.0V~3.3V~3.6V	
	Azalia Codec: ALC262		
	Azalia MDC:		
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC	2V~3.3V~3.465V	6uA
	ICH9M:VCCSUS3_3	3.135V~3.3V~3.465V	212mA
	ICH9M:VCCCL3_3	3.135V~3.3V~3.465V	73mA
	ICH9M:VCCLAN3_3	3.135V~3.3V~3.465V	78mA
	LCD:	3.0V~3.3V~3.6V	2A
	Lan:AR8131	3.0V~3.3V~3.6V	1A
	Azalia MDC:		
	Flash ROM: BIOS	3.0V~3.3V~3.6V	
5VS	Cardreader: RTS5159	3.0V~3.3V~3.6V	
	Azalia Codec: ALC269	3.0V~3.3V~3.6V	
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA
	~~ODD: SATA~~	~~4.75V~5.0V~5.25V~~	~~Max: 1.5A ; R/W: 900mA ; STDBY: 45mA~~
	~~Audio AMP: G1432~~		
	Inverter:		
	WebCam	4.75V~5.0V~5.25V	1A
5VA	USB: x 2 ports	5VA	2A
	USB	5VA	1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

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TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF
ANNOTATIONS

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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CHANGE by Miles Liu DATE Tuesday, March 10, 2009

6.Schematic modify Item and History :

2009.0108

1. ADD USB P3 for Docking, USB P5 for Finger printer,
   Modify CN5 -----P28
2. Modify CN20 to 50pin-------P33
3. Move PWR_SWIN# from CN14 to CN20
4. ADD TPM module------P34

2009.0109

1. ADD DOCK_USB_EN, DOCK_CRT_IN#-----P32,33

2009.0112

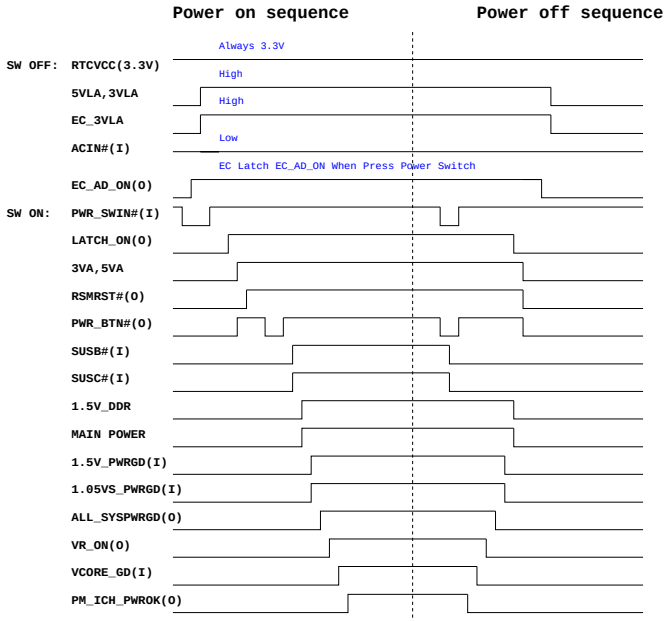
1. Change power item: R490,R291,BAT CNN TH PIN

INVENTEC			
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF Schematic Modify			
SIZE Custom	CODE X01	DOC.NUMBER D-CS-1310A2264501-ALG	REV X01
CHANGE by Miles Liu	DATE Tuesday, March 10, 2009	SHEET	

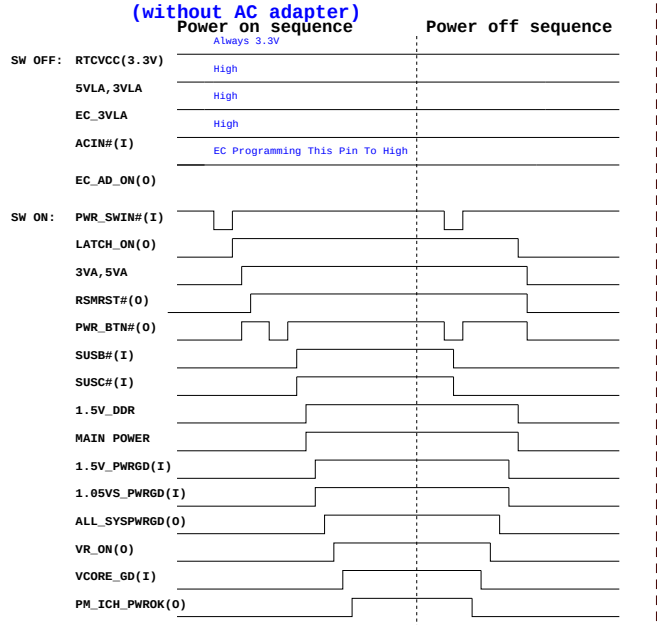
SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

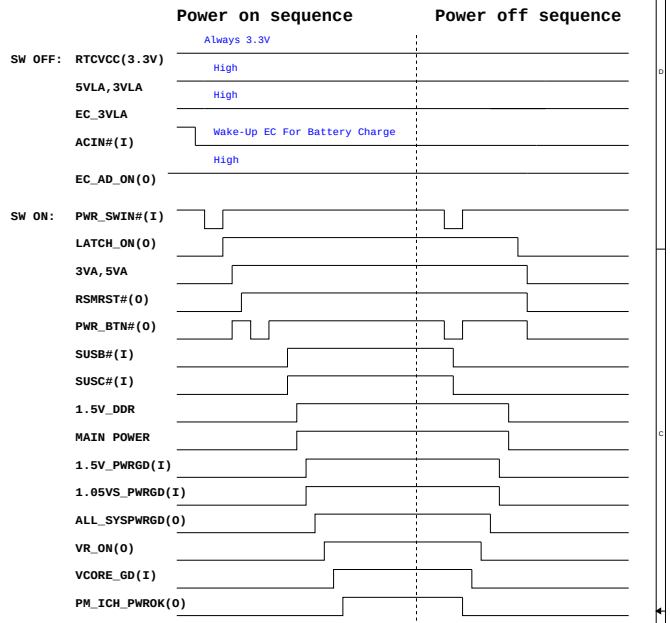
Power on/off sequence AC insert (without Battery Pack)



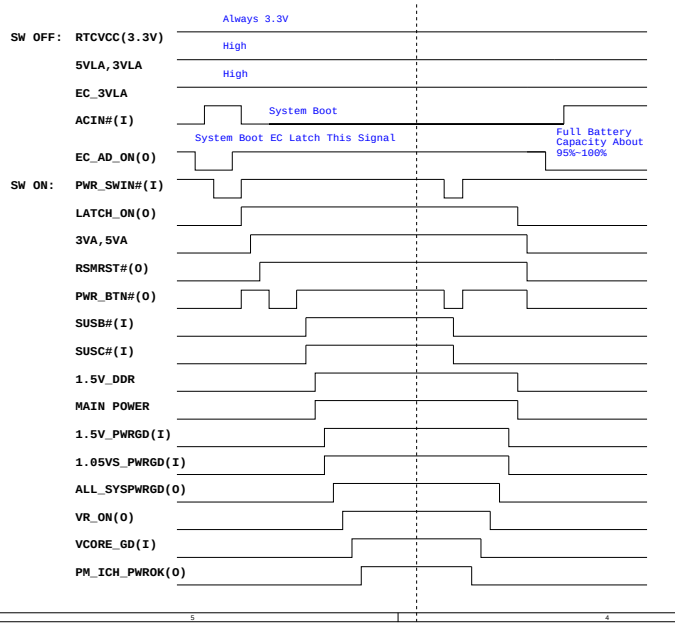
Power on/off sequence Battery insert (without AC adapter)



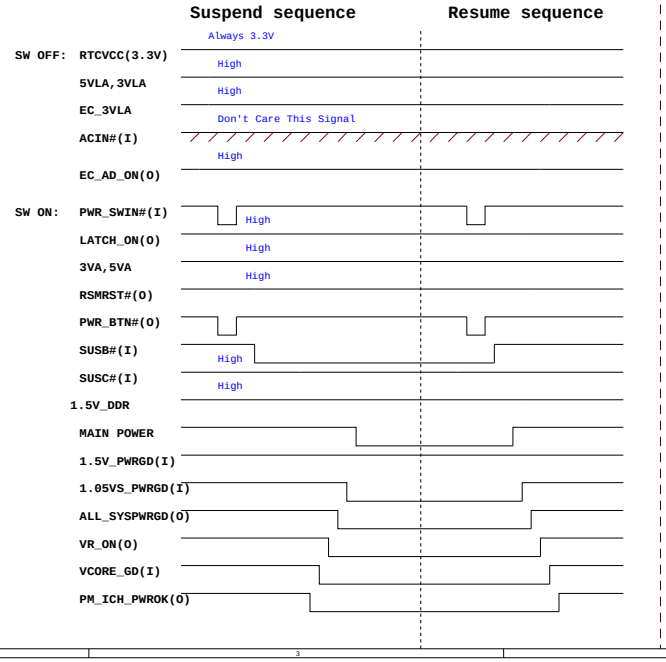
Power on/off sequence AC insert(with charge over 95%)



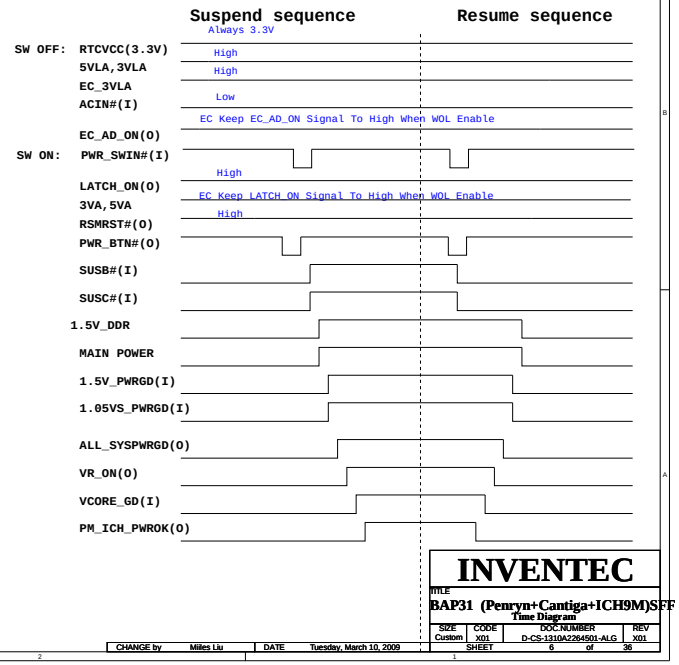
Power on/off sequence AC insert(without charge over 95%)



Suspend And Resume Sequence (S3)



Power on/off sequence after windows shoutdown (WOL enable)



INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
Time Diagram

SIZE	CODE	DOC NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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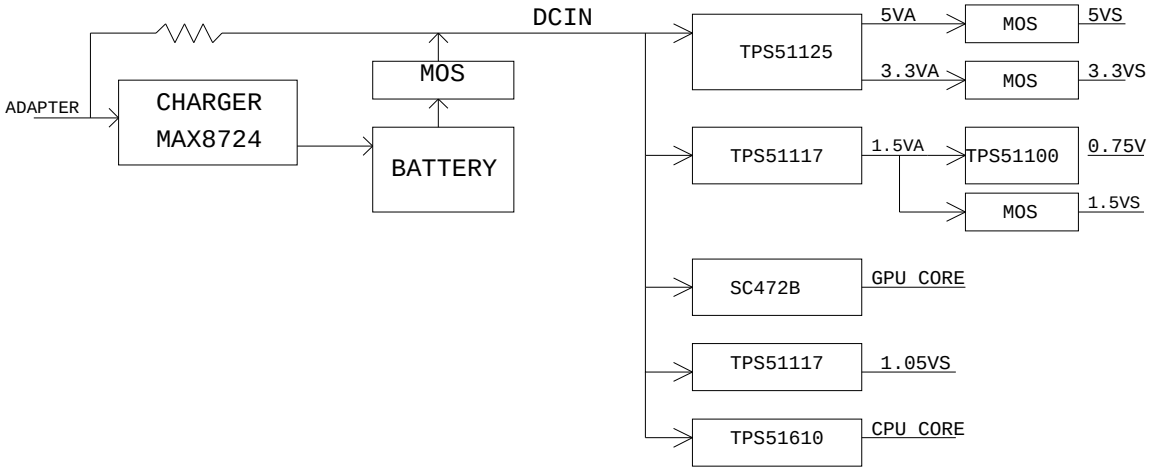
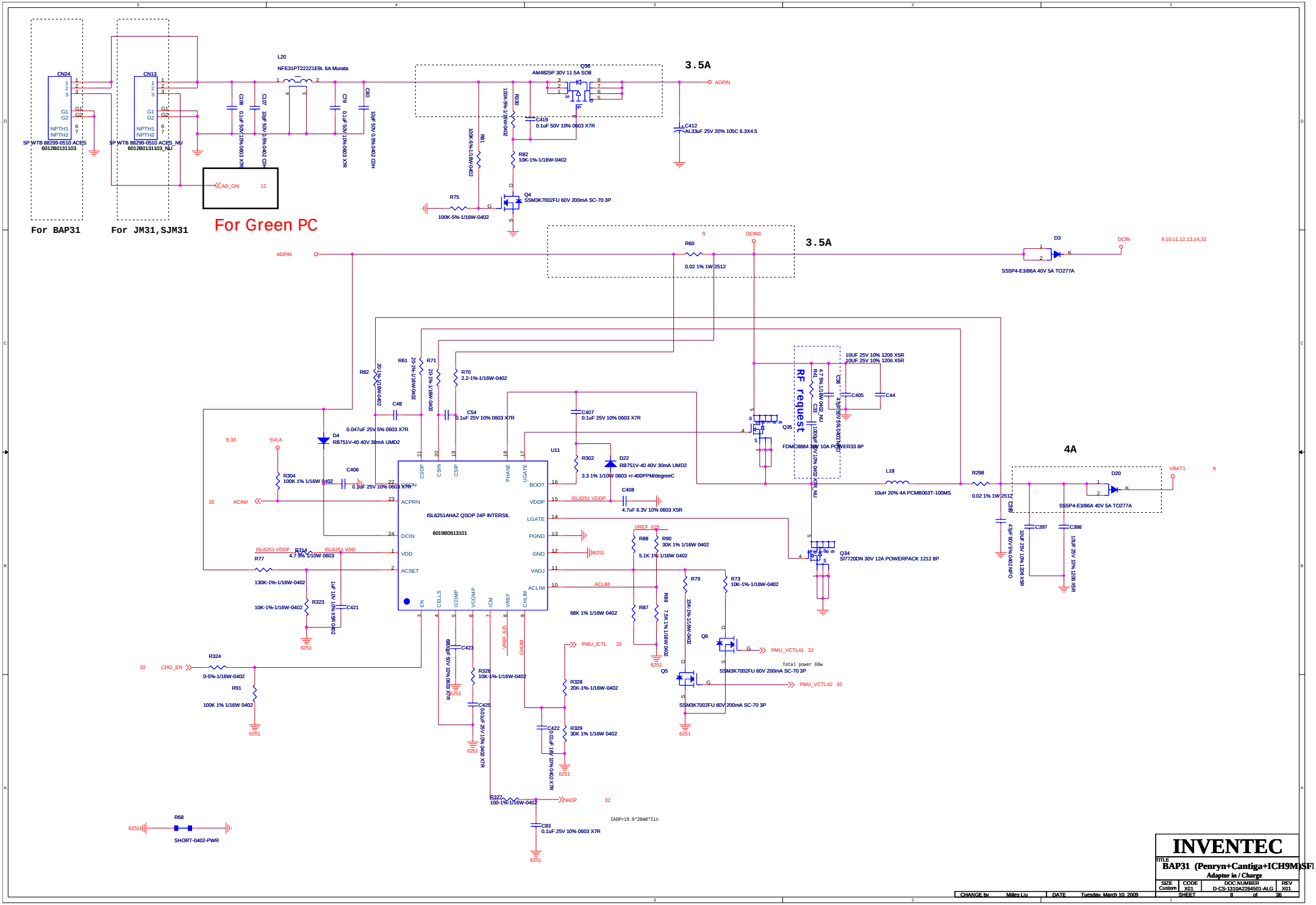
CHANGE by	Milles Liu	DATE	Tuesday, March 10, 2009

Power Block Diagram :



INVENTEC			
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF Power Block Diagram			
SIZE C	CODE X01	DOC.NUMBER D-CS-1310A2264501-ALG	REV X01
		SHEET	

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009


CN24
5P WTB 88298-0610 ACES
6012B0131103
CN13
5P WTB 88298-0610 ACES_NU
6012B0131103_NU
For BAP31
For JM31,SJM31
For Green PC
AD_ON
L20
NFE31PT222Z1E9L 6A Murata
Q36
AM4825P 30V 11.5A SO8
3.5A
ADPIN
C412
AL33uF 25V 20% 105C 6.3X4.5
C419
0.1uF 50V 10% 0603 X7R
R82
10K-1%-1/16W-0402
Q4
SSM3K7002FU 60V 200mA SC-70 3P
R75
100K-5%-1/16W-0402
R60
0.02 1% 1W 2512
DCIN0
D3
SS5P4-E3/86A 40V 5A TO277A
DCIN
9,10,11,12,13,14,31
R62
20-1%-1/16W-0402
R61
20-1%-1/16W-0402
R71
20-1%-1/16W-0402
R70
2.2-1%-1/16W-0402
C48
0.047uF 25V 5% 0603 X7R
C54
0.1uF 25V 10% 0603 X7R
C407
0.1uF 25V 10% 0603 X7R
D4
RB751V-40 40V 30mA UMD2
5VLA
R304
100K 1% 1/16W 0402
C406
0.1uF 25V 10% 0603 X7R
U11
ISL6251AHAZ QSOP 24P INTERSIL
6019B0613101
CSOP
CSIN
CSIP
PHASE
UGATE
BOOT
VDDP
LGATE
PGND
GND
VADJ
ACLIM
CHLIM
EN
CELLS
ICOMP
VCOMP
ICM
VREF
ACPRN
DCIN
VDD
ACSET
ACIN#
R302
3.3 1% 1/10W 0603 +/-400PPM/degreeC
D22
RB751V-40 40V 30mA UMD2
ISL6251 VDDP
C408
4.7uF 6.3V 10% 0603 X5R
RF request
Q35
FDMC8884 30V 10A POWER33 8P
10UF 25V 10% 1206 X5R
10UF 25V 10% 1206 X5R
C405
C44
L18
10uH 20% 4A PCMB063T-100MS
R298
0.02 1% 1W 2512
4A
D20
SS5P4-E3/86A 40V 5A TO277A
VBAT1
C397
C398
Q34
SI7720DN 30V 12A POWERPACK 1212 8P
R314
4.7 5% 1/10W 0603
ISL6251 VDD
R77
130K-1%-1/16W-0402
R323
10K-1%-1/16W-0402
C421
1uF 10V 10% X5R 0402
VREF 625
R88
R90
30K 1% 1/16W 0402
5.1K 1% 1/16W 0402
R87
68K 1% 1/16W 0402
R89
7.5K 1% 1/16W 0402
R79
15K-1%-1/16W-0402
R73
10K-1%-1/16W-0402
Q6
SSM3K7002FU 60V 200mA SC-70 3P
Q5
SSM3K7002FU 60V 200mA SC-70 3P
PMU_VCTL41
PMU_VCTL42
Total power 60w
PMU_ICTL
R324
0-5%-1/16W-0402
R91
100K 1% 1/16W 0402
CHG_EN
C423
R326
10K-1%-1/16W-0402
C425
0.01uF 25V 10% 0402 X7R
R328
20K-1%-1/16W-0402
C422
0.01uF 16V 10% 0402 X7R
R329
30K 1% 1/16W 0402
R327
100-1%-1/16W-0402
IADP
C83
0.1uF 25V 10% 0603 X7R
IADP=19.9*20mR*Iin
R68
SHORT-0402-PWR
6251
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
Adaptor in / Charge
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
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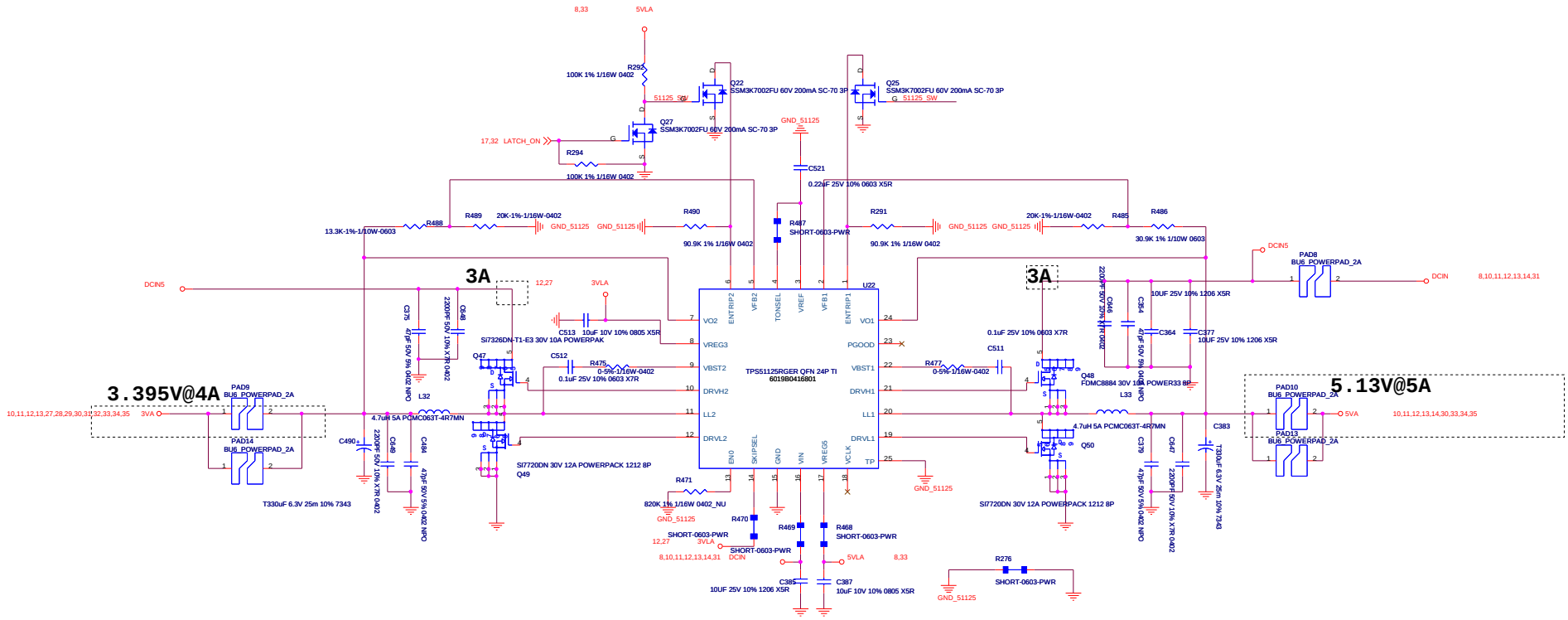
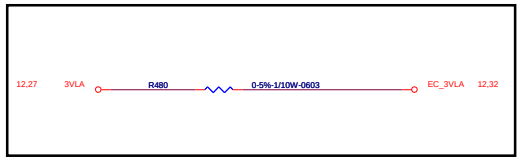
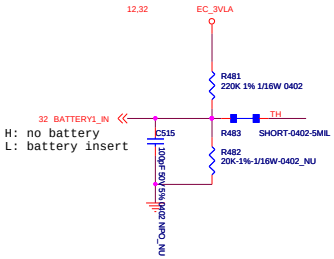
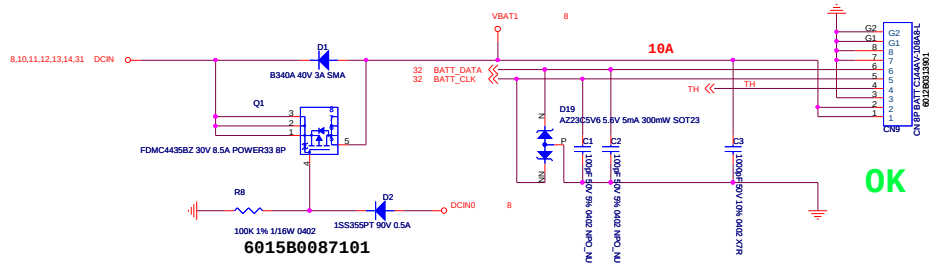
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009



For Green PC







INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
5VLA/5VA/3VLA/3VA

SIZE Custom

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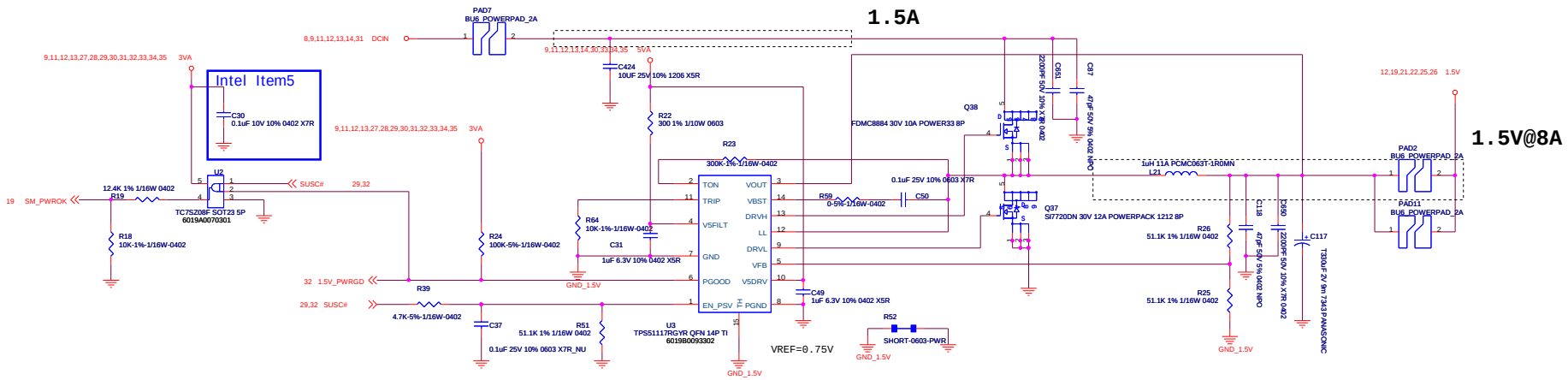

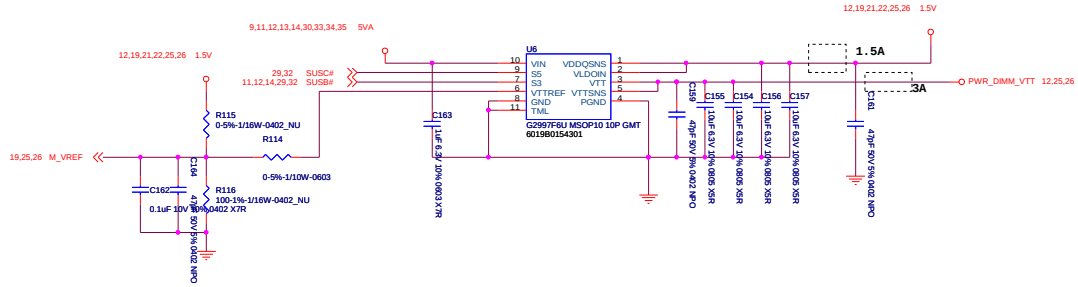

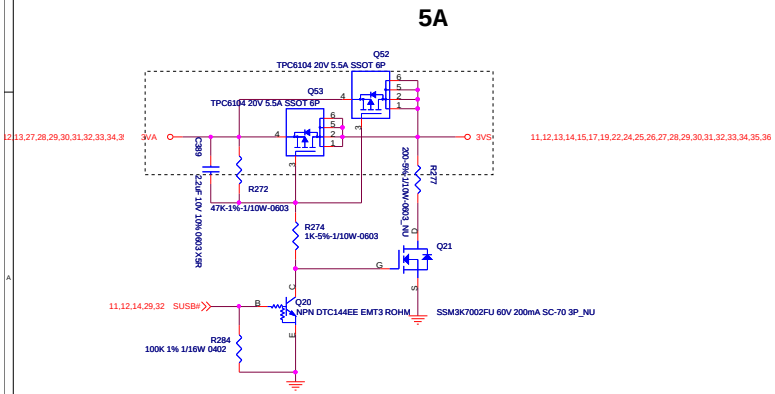

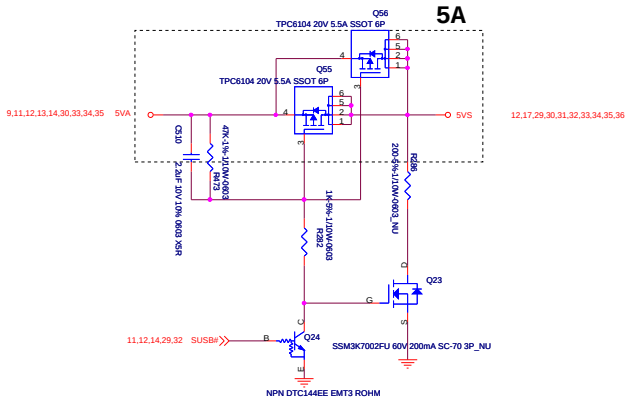

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
3VS/5VS/1.5V (DDR3)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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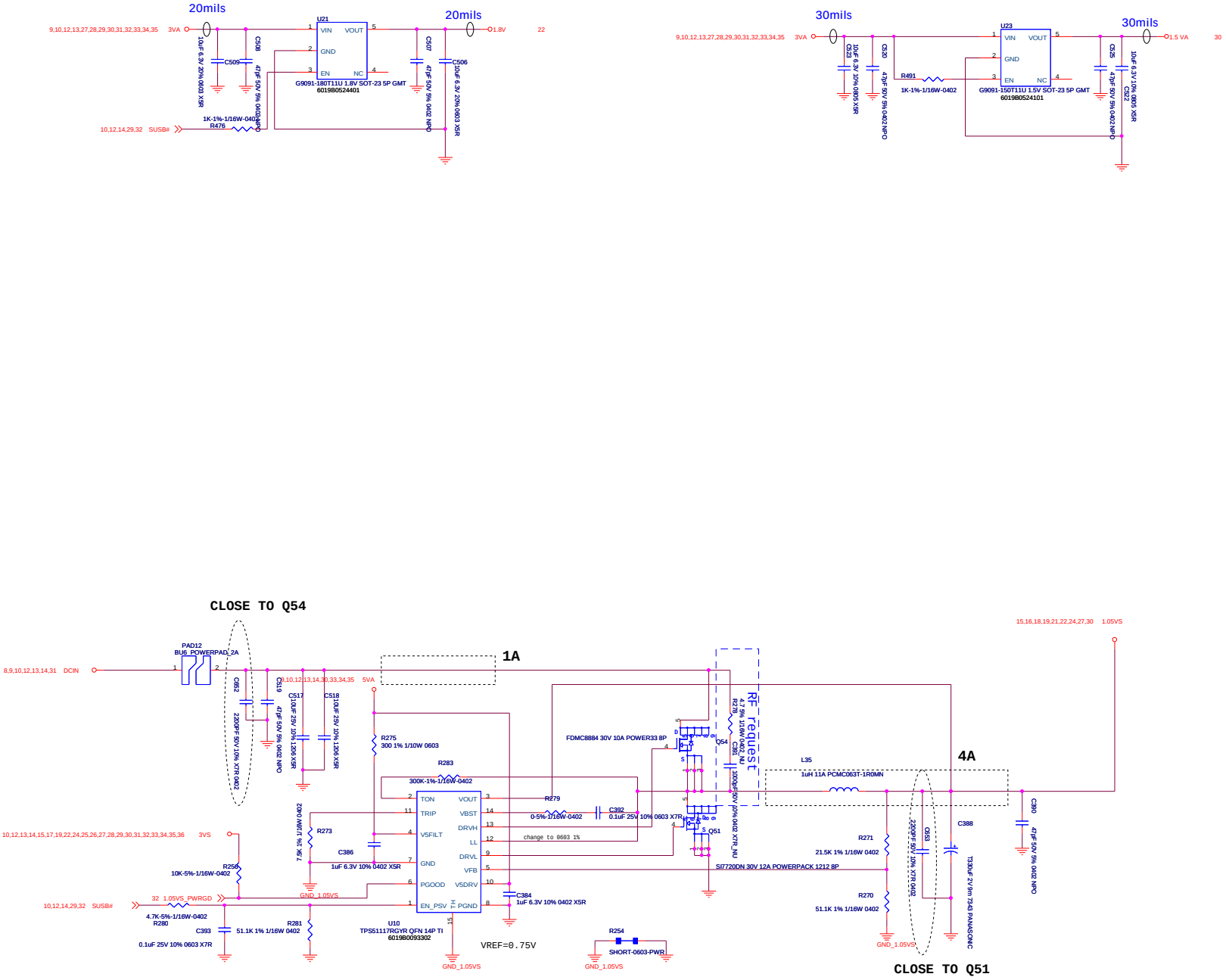
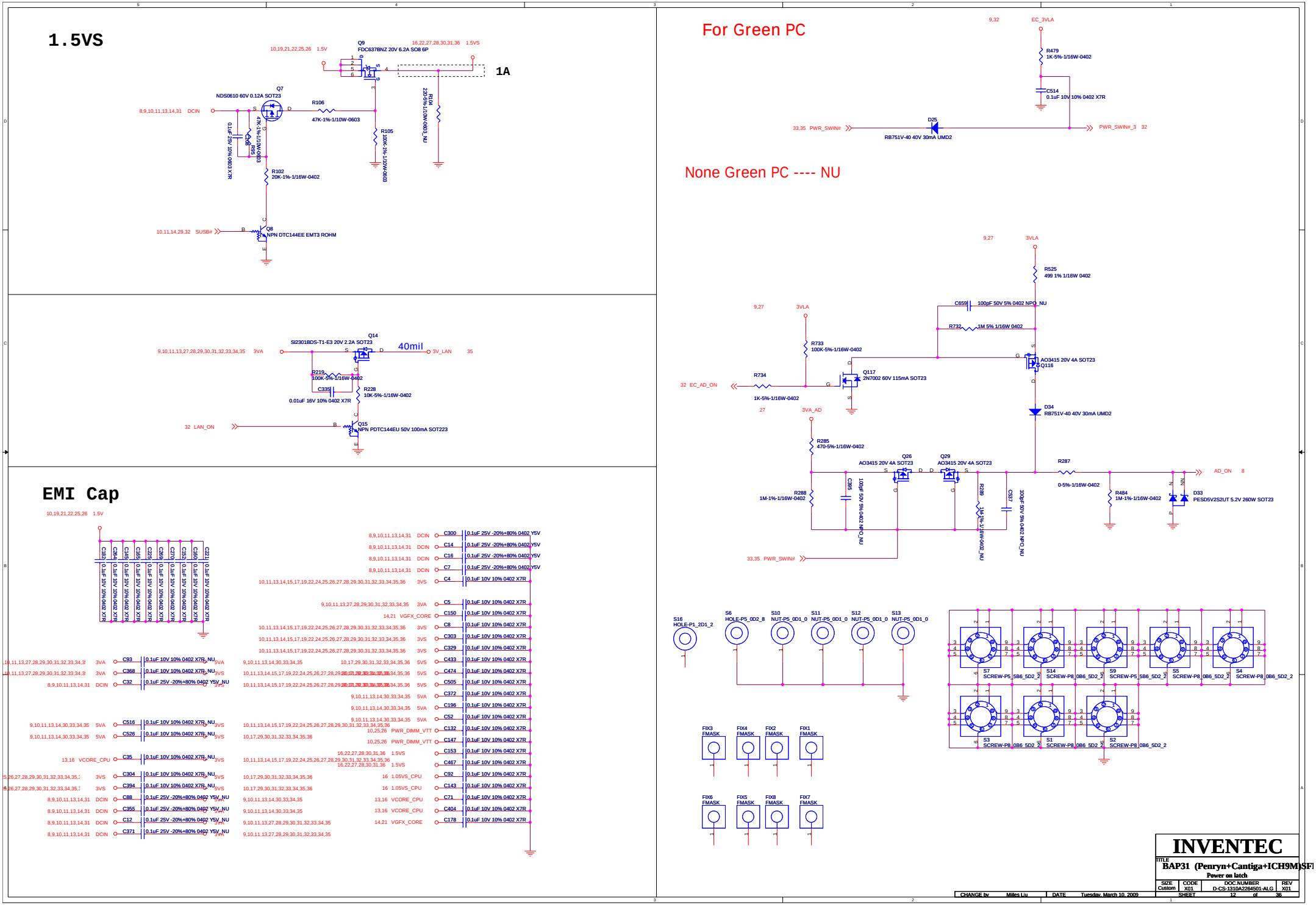


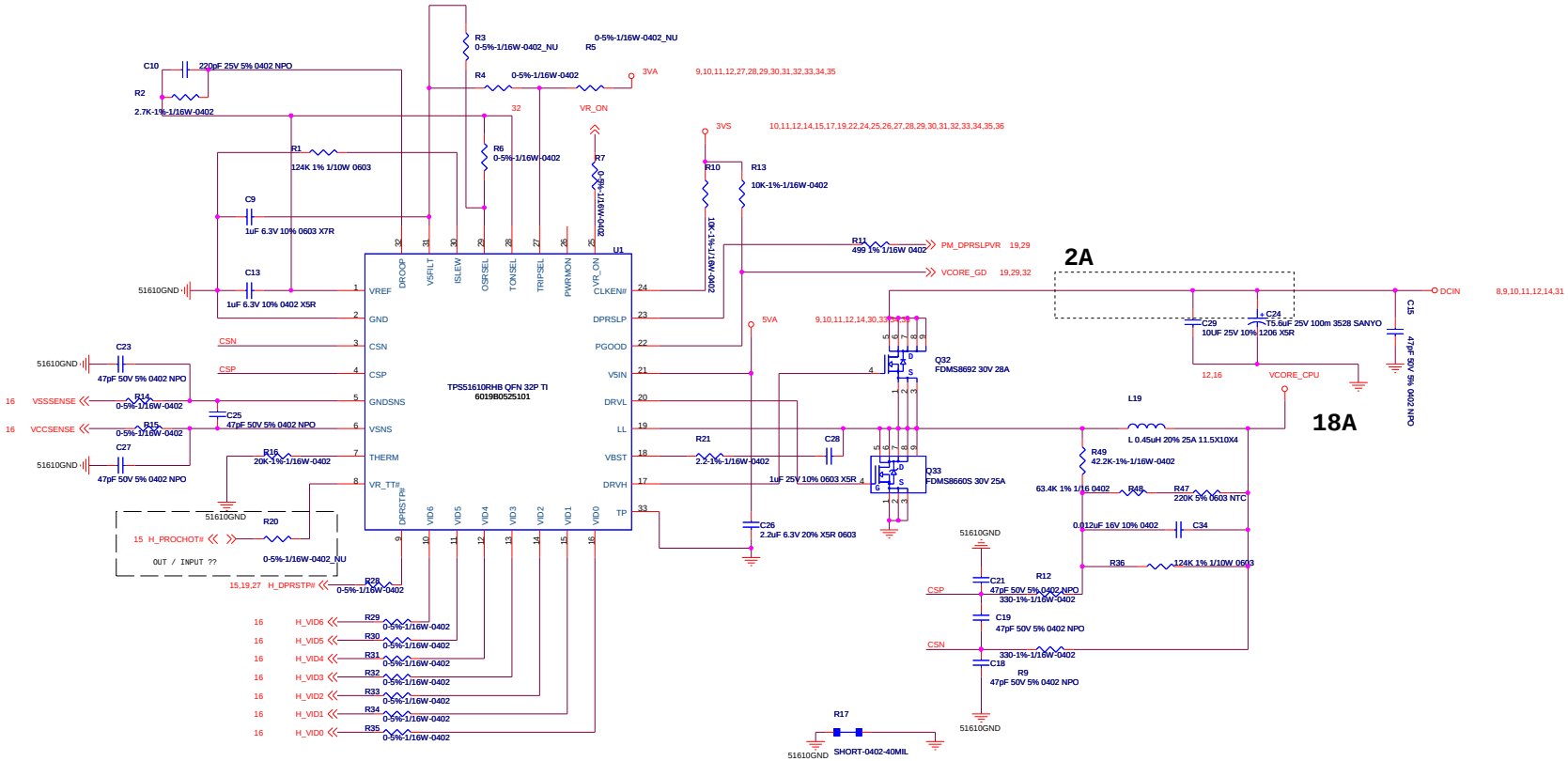
INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
1.05VS/1.5S/1.8V/1.5VA

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009


1.5VS
10,19,21,22,25,26 1.5V
Q9
FDC637BNZ 20V 6.2A SO8 6P
16,22,27,28,30,31,36 1.5VS
1A
Q7
NDS0610 60V 0.12A SOT23
8,9,10,11,13,14,31 DCIN
R106
47K-1%-1/10W-0603
R105
100K-1%-1/10W-0603
R104
230-5%-1/10W-0603_NU
0.1uF 25V 10% 0603 X7R
R103
4.7K-1%-1/10W-0603
R102
20K-1%-1/16W-0402
10,11,14,29,32 SUSB#
Q8
NPN DTC144EE EMT3 ROHM
9,10,11,13,27,28,29,30,31,32,33,34,35 3VA
Q14
SI2301BDS-T1-E3 20V 2.2A SOT23
40mil
3V_LAN 35
R219
100K-5%-1/16W-0402
C335
0.01uF 16V 10% 0402 X7R
R228
10K-5%-1/16W-0402
32 LAN_ON
Q15
NPN PDTC144EU 50V 100mA SOT223
EMI Cap
10,19,21,22,25,26 1.5V
C182 0.1uF 10V 10% 0402 X7R
C284 0.1uF 10V 10% 0402 X7R
C145 0.1uF 10V 10% 0402 X7R
C185 0.1uF 10V 10% 0402 X7R
C225 0.1uF 10V 10% 0402 X7R
C269 0.1uF 10V 10% 0402 X7R
C270 0.1uF 10V 10% 0402 X7R
C152 0.1uF 10V 10% 0402 X7R
C160 0.1uF 10V 10% 0402 X7R
C221 0.1uF 10V 10% 0402 X7R
C93 0.1uF 10V 10% 0402 X7R_NU
C368 0.1uF 10V 10% 0402 X7R_NU
C32 0.1uF 25V -20%+80% 0402 Y5V_NU
C516 0.1uF 10V 10% 0402 X7R_NU
C526 0.1uF 10V 10% 0402 X7R_NU
C35 0.1uF 10V 10% 0402 X7R_NU
C304 0.1uF 10V 10% 0402 X7R_NU
C394 0.1uF 10V 10% 0402 X7R_NU
C88 0.1uF 25V -20%+80% 0402 Y5V_NU
C355 0.1uF 25V -20%+80% 0402 Y5V_NU
C12 0.1uF 25V -20%+80% 0402 Y5V_NU
C371 0.1uF 25V -20%+80% 0402 Y5V_NU
C300 0.1uF 25V -20%+80% 0402 Y5V
C14 0.1uF 25V -20%+80% 0402 Y5V
C16 0.1uF 25V -20%+80% 0402 Y5V
C7 0.1uF 25V -20%+80% 0402 Y5V
C4 0.1uF 10V 10% 0402 X7R
C5 0.1uF 10V 10% 0402 X7R
C150 0.1uF 10V 10% 0402 X7R
C8 0.1uF 10V 10% 0402 X7R
C303 0.1uF 10V 10% 0402 X7R
C329 0.1uF 10V 10% 0402 X7R
C433 0.1uF 10V 10% 0402 X7R
C474 0.1uF 10V 10% 0402 X7R
C505 0.1uF 10V 10% 0402 X7R
C372 0.1uF 10V 10% 0402 X7R
C196 0.1uF 10V 10% 0402 X7R
C52 0.1uF 10V 10% 0402 X7R
C132 0.1uF 10V 10% 0402 X7R
C147 0.1uF 10V 10% 0402 X7R
C153 0.1uF 10V 10% 0402 X7R
C467 0.1uF 10V 10% 0402 X7R
C92 0.1uF 10V 10% 0402 X7R
C143 0.1uF 10V 10% 0402 X7R
C71 0.1uF 10V 10% 0402 X7R
C404 0.1uF 10V 10% 0402 X7R
C178 0.1uF 10V 10% 0402 X7R
For Green PC
9,32 EC_3VLA
R479
1K-5%-1/16W-0402
C514
0.1uF 10V 10% 0402 X7R
D25
RB751V-40 40V 30mA UMD2
33,35 PWR_SWIN#
PWR_SWIN#_3 32
None Green PC ---- NU
9,27 3VLA
R525
499 1% 1/16W 0402
C659 100pF 50V 5% 0402 NPO NU
R732 1M 5% 1/16W 0402
R733
100K-5%-1/16W-0402
Q117
2N7002 60V 115mA SOT23
AO3415 20V 4A SOT23
Q116
R734
1K-5%-1/16W-0402
32 EC_AD_ON
D34
RB751V-40 40V 30mA UMD2
27 3VA_AD
R285
470-5%-1/16W-0402
Q26
AO3415 20V 4A SOT23
Q29
AO3415 20V 4A SOT23
R287
0-5%-1/16W-0402
AD_ON 8
R288
1M-1%-1/16W-0402
C395
100pF 50V 5% 0402 NPO_NU
R289
1M-1%-1/16W-0402_NU
C397
100pF 50V 5% 0402 NPO_NU
R484
1M-1%-1/16W-0402
D33
PESD5V2S2UT 5.2V 260W SOT23
33,35 PWR_SWIN#
S16
HOLE-P1_2D1_2
S6
HOLE-P5_0D2_8
S10
NUT-P5_0D1_0
S11
NUT-P5_0D1_0
S12
NUT-P5_0D1_0
S13
NUT-P5_0D1_0
S7
SCREW-P5_5B6_5D2_2
S14
SCREW-P8_0B6_5D2_2
S9
SCREW-P5_5B6_5D2_2
S5
SCREW-P8_0B6_5D2_2
S4
SCREW-P8_0B6_5D2_2
S3
SCREW-P8_0B6_5D2_2
S1
SCREW-P8_0B6_5D2_2
S2
SCREW-P8_0B6_5D2_2
FIX3
FMASK
FIX4
FMASK
FIX2
FMASK
FIX1
FMASK
FIX6
FMASK
FIX5
FMASK
FIX8
FMASK
FIX7
FMASK
INVENTEC
TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFI
Power on latch
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
SHEET 12 of 36
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009



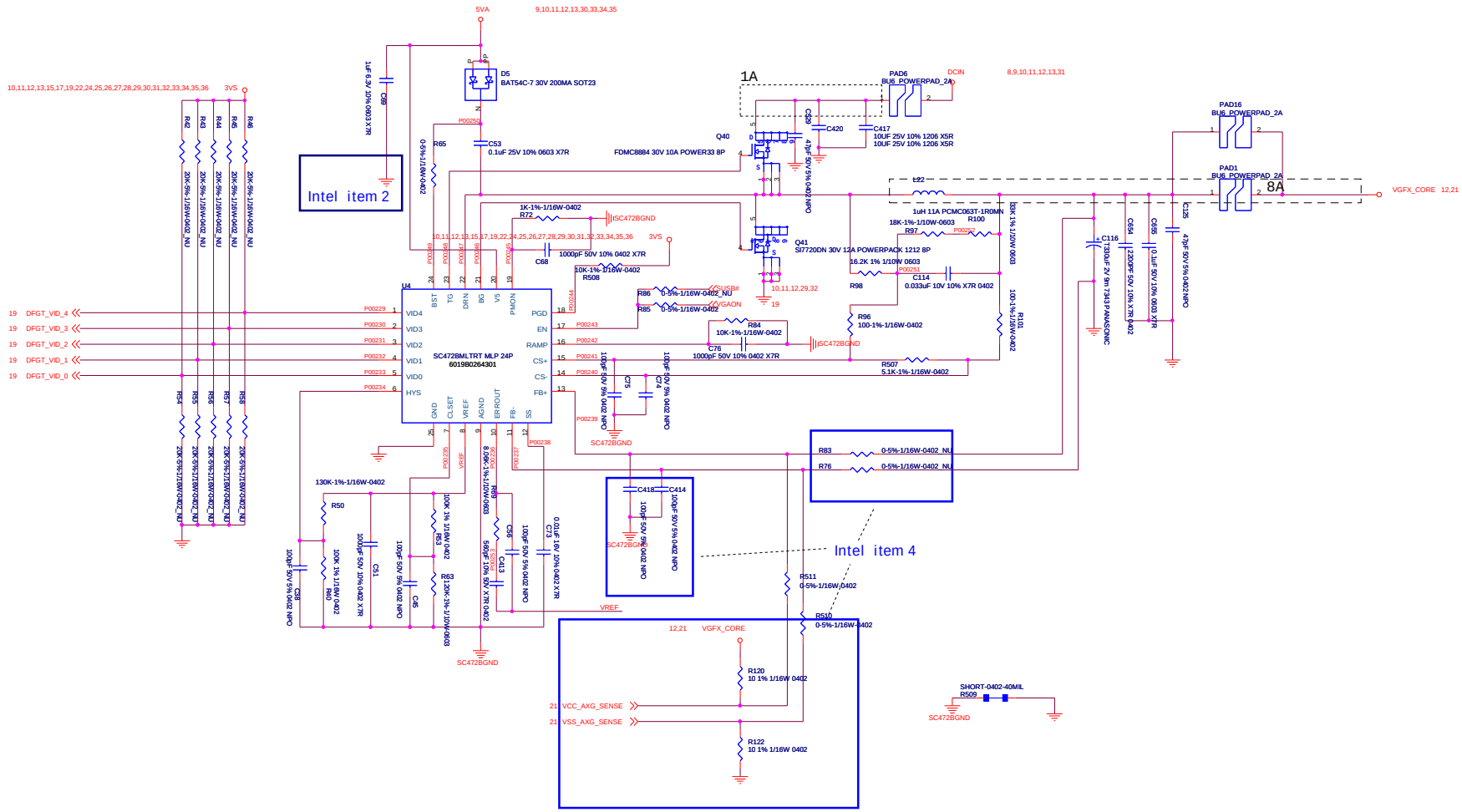
INVENTEC

TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF
CPU Core Power

SIZE	CODE	DOC.NUMBER
C	X01	D-CS-1310A2264501-ALG

SHEET 13 of

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009



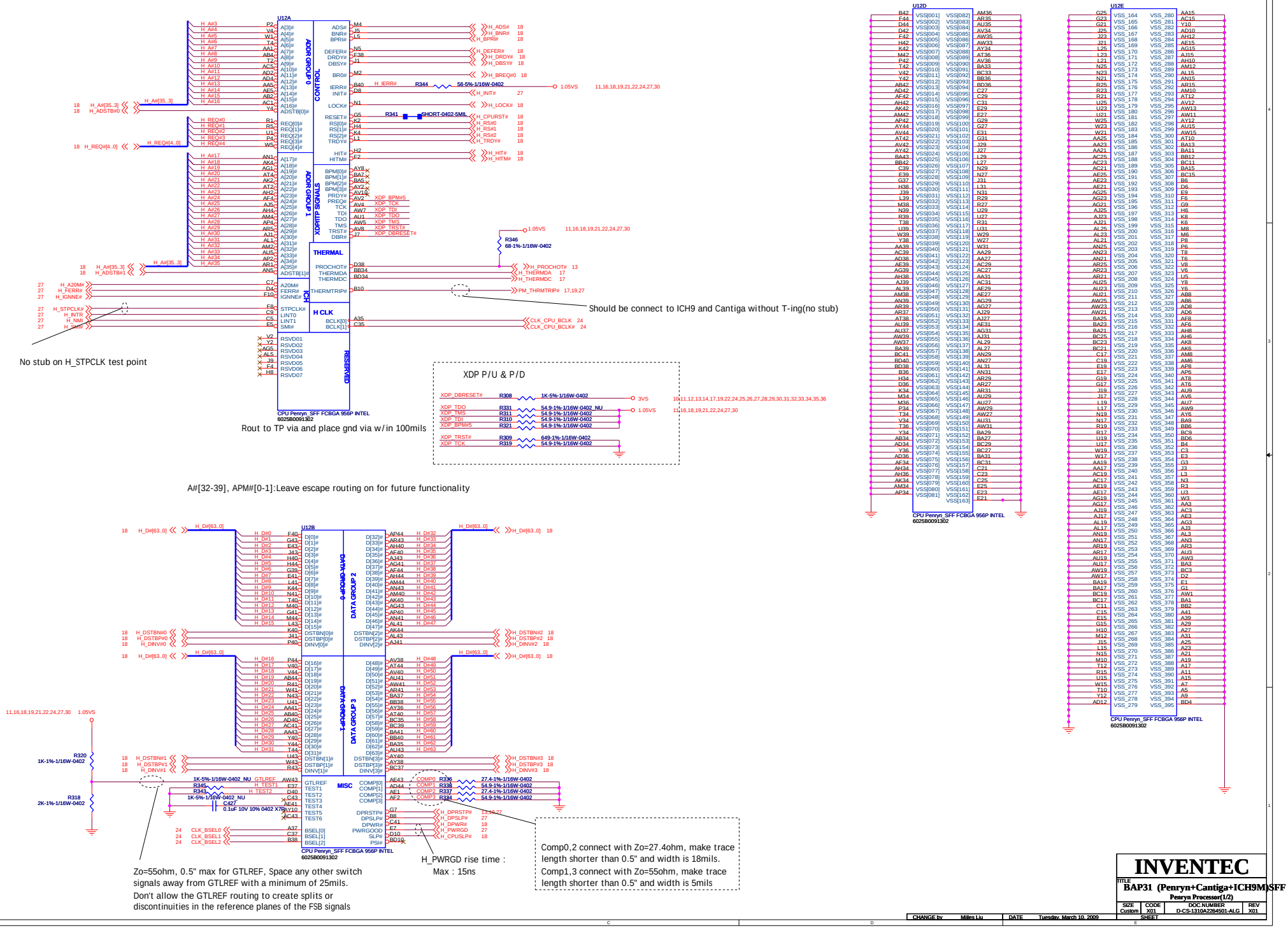
INVENTEC

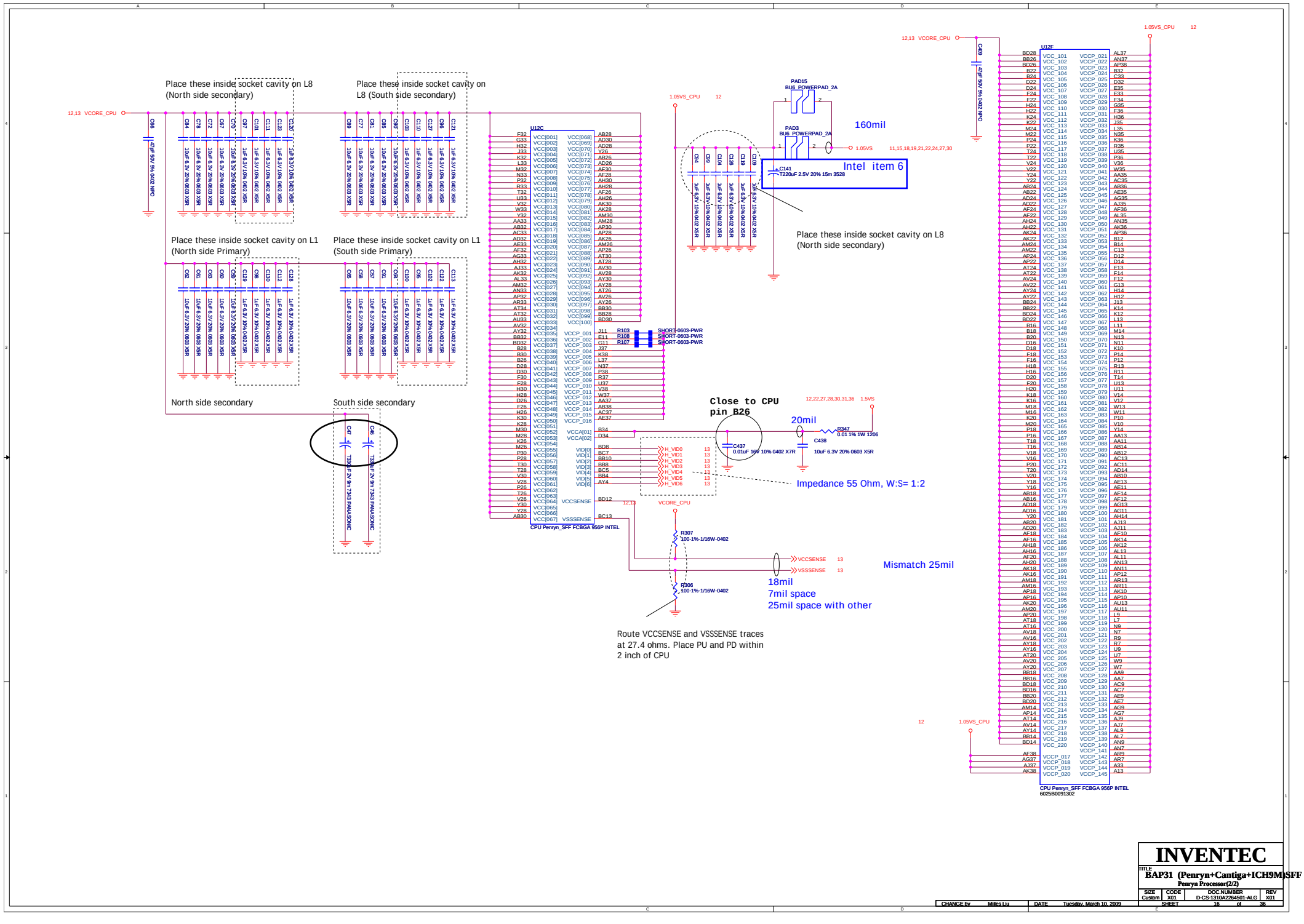
TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
GPU CORE

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

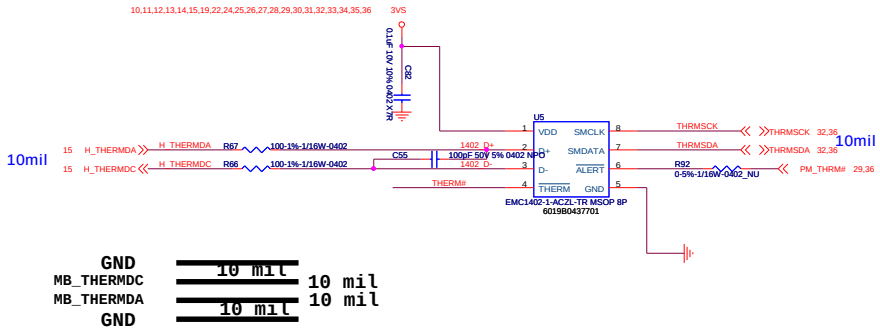
SHEET 14 of 36

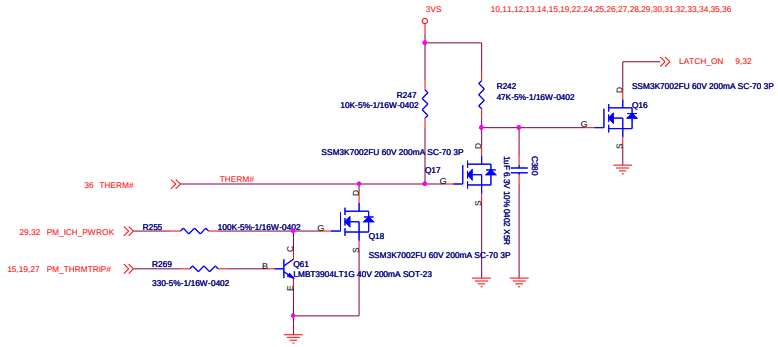
CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009


U12A
U12B
U12D
U12E
CPU Penryn_SFF FCBGA 956P INTEL
6025B0091302
R344 56-5%-1/16W-0402
R341 SHORT-0402-5MIL
R346 68-1%-1/16W-0402
THERMAL
H CLK
XDP P/U & P/D
R308 1K-5%-1/16W-0402
R331 54.9-1%-1/16W-0402_NU
R311 54.9-1%-1/16W-0402
R310 54.9-1%-1/16W-0402
R321 54.9-1%-1/16W-0402
R309 649-1%-1/16W-0402
R319 54.9-1%-1/16W-0402
R320 1K-1%-1/16W-0402
R318 2K-1%-1/16W-0402
R345 1K-5%-1/16W-0402_NU
R343 1K-5%-1/16W-0402_NU
C427 0.1uF 10V 10% 0402 X7R
R336 27.4-1%-1/16W-0402
R338 54.9-1%-1/16W-0402
R337 27.4-1%-1/16W-0402
R334 54.9-1%-1/16W-0402
No stub on H_STPCLK test point
Should be connect to ICH9 and Cantiga without T-ing(no stub)
Rout to TP via and place gnd via w/in 100mils
A#[32-39], APM#[0-1]:Leave escape routing on for future functionality
Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils.
Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals
H_PWRGD rise time : Max : 15ns
Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils.
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils
INVENTEC
TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
Penryn Processor(1/2)
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
SHEET
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009

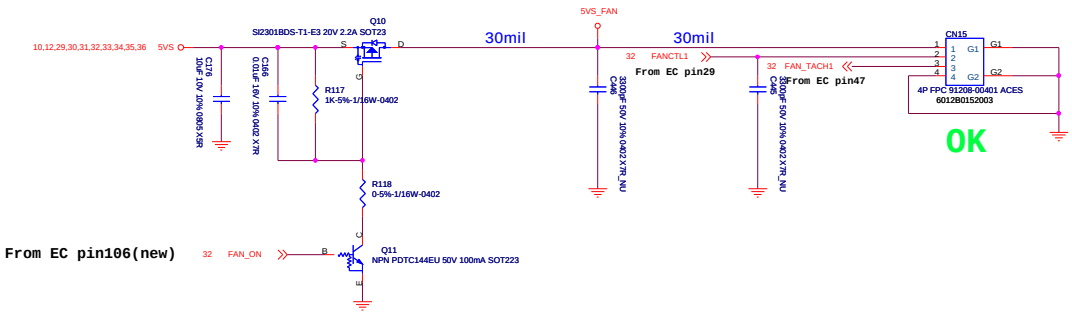

Place these inside socket cavity on L8 (North side secondary)
Place these inside socket cavity on L8 (South side secondary)
Place these inside socket cavity on L1 (North side Primary)
Place these inside socket cavity on L1 (South side Primary)
North side secondary
South side secondary
12,13 VCORE_CPU
1.05VS_CPU 12
U12C
CPU Penryn_SFF FCBGA 956P INTEL
PAD15 BU6_POWERPAD_2A
PAD3 BU6_POWERPAD_2A
160mil
1.05VS 11,15,18,19,21,22,24,27,30
Intel item 6
C141 T220uF 2.5V 20% 15m 3528
Place these inside socket cavity on L8 (North side secondary)
SHORT-0603-PWR
Close to CPU pin B26
12,22,27,28,30,31,36 1.5VS
20mil
R347 0.01 1% 1W 1206
C437 0.01uF 16V 10% 0402 X7R
C438 10uF 6.3V 20% 0603 X5R
Impedance 55 Ohm, W:S= 1:2
VCORE_CPU
R307 100-1%-1/16W-0402
R306 100-1%-1/16W-0402
VCCSENSE 13
VSSSENSE 13
Mismatch 25mil
18mil
7mil space
25mil space with other
Route VCCSENSE and VSSSENSE traces at 27.4 ohms. Place PU and PD within 2 inch of CPU
U12F
CPU Penryn_SFF FCBGA 956P INTEL
6025B0091302
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
Penryn Processor(2/2)
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
SHEET 16 of 36
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009

THERMAL SENSOR





Fan control



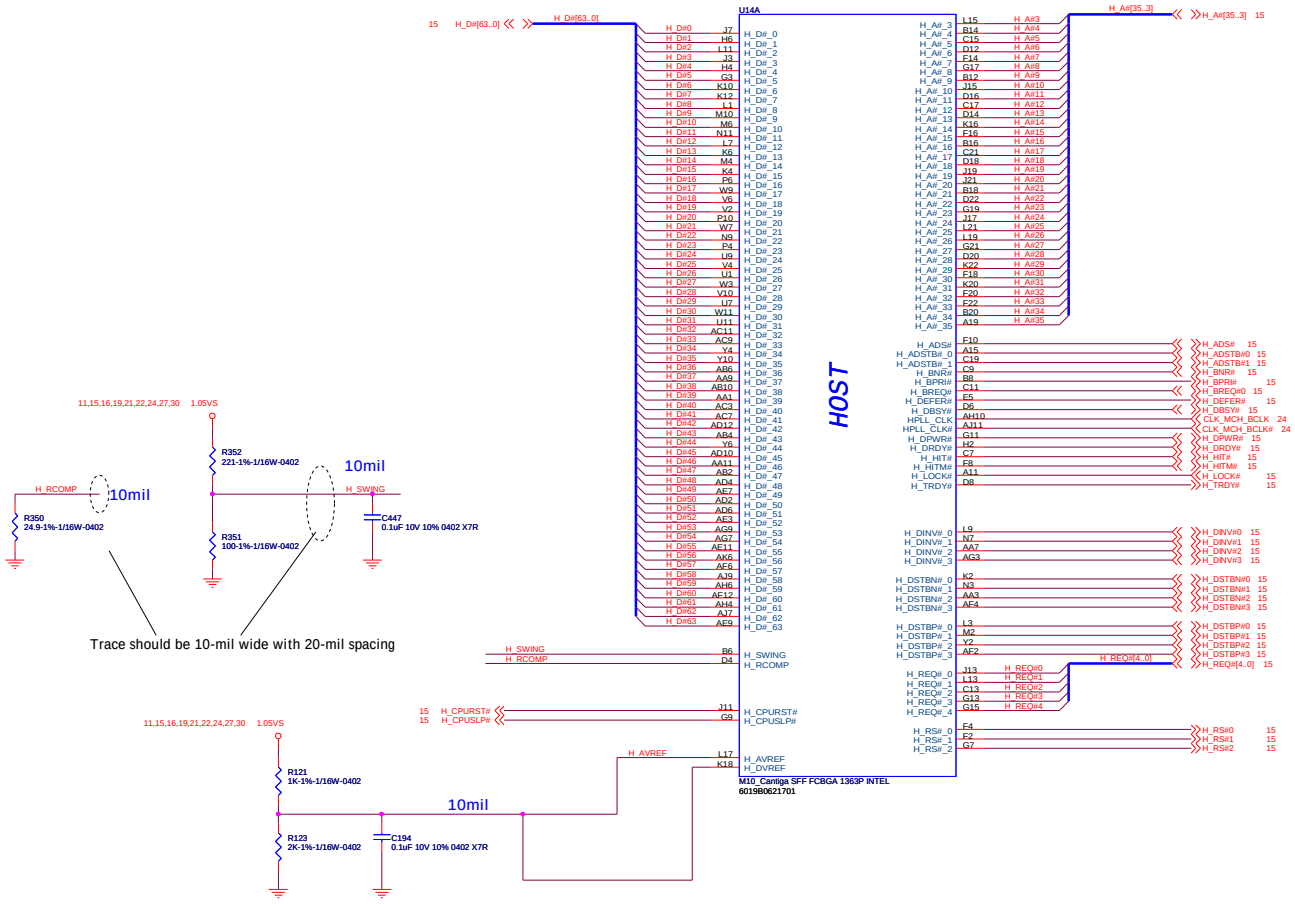
CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
CPU Thermal

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET



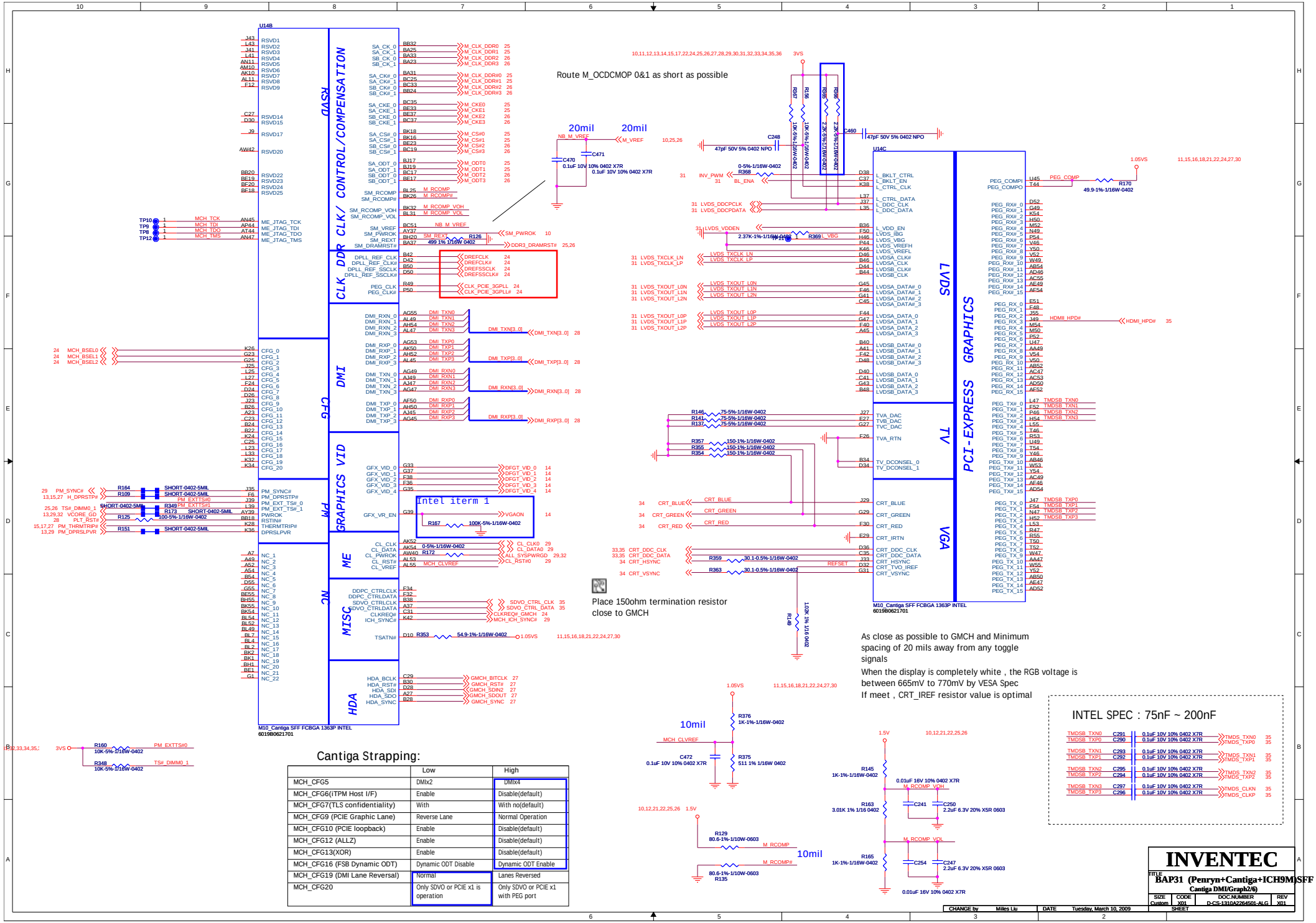
INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Host(1/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A226-6501-ALG	X01

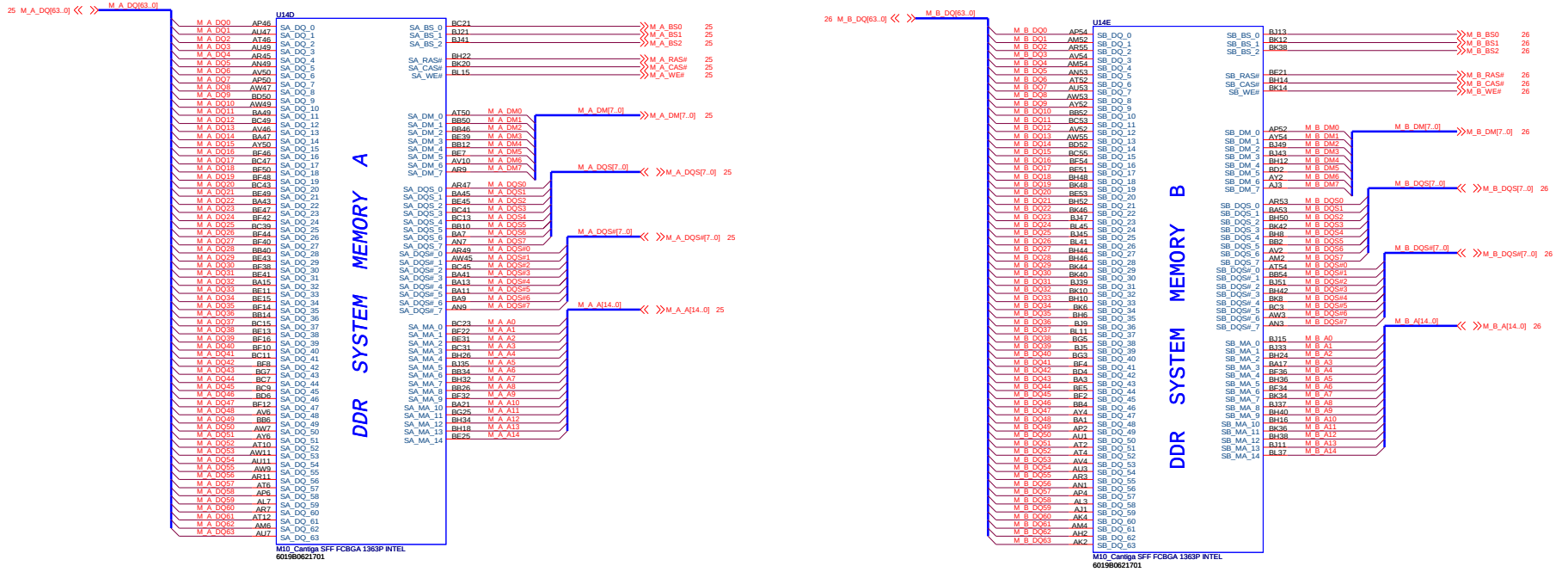
SHEET 18 of 36

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009



Cantiga Strapping:

	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(iTPM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIE loopback)	Enable	Disable(default)
MCH_CFG12 (ALLZ)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIE x1 is operation	Only SDVO or PCIE x1 with PEG port



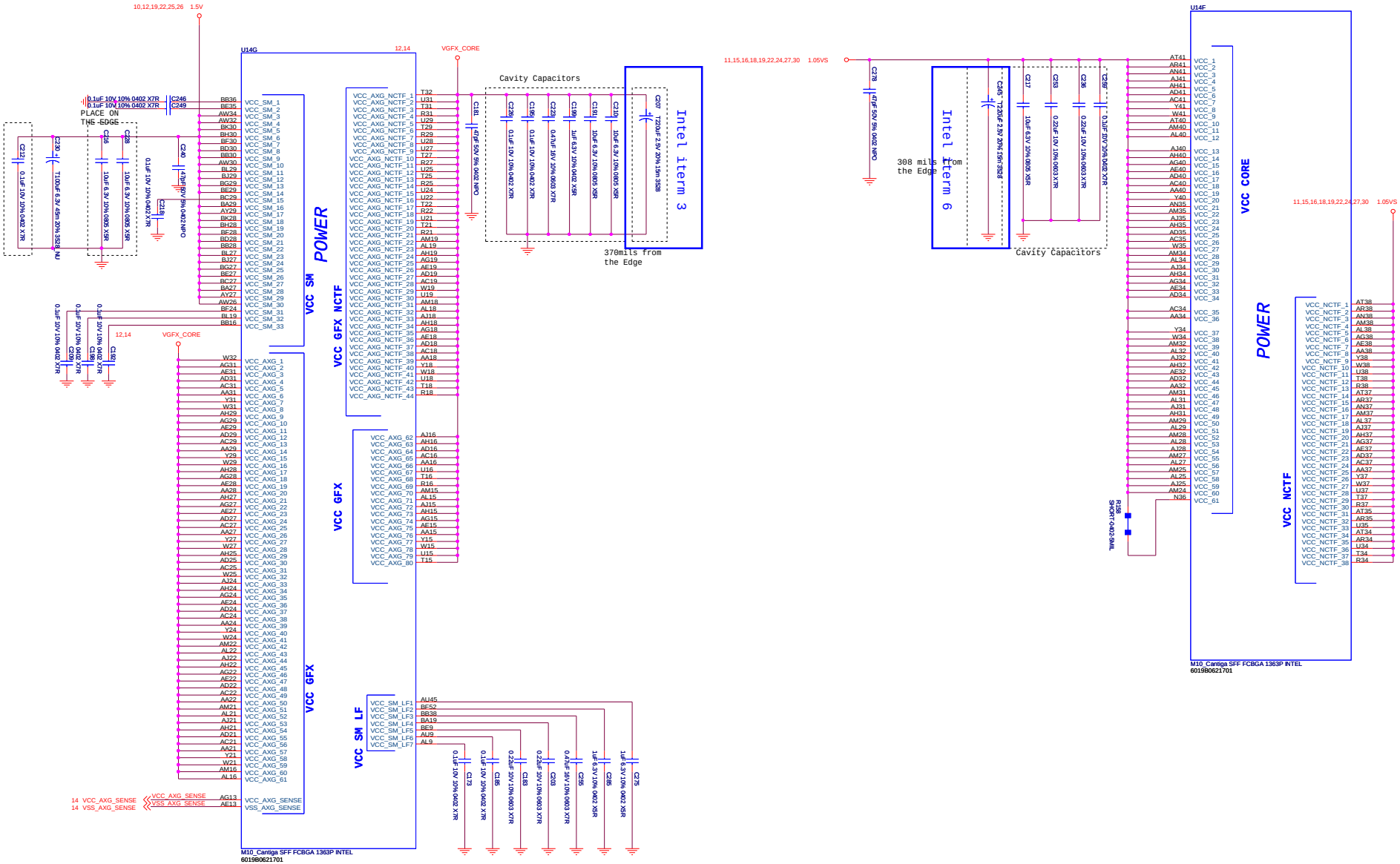
CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

INVENTEC

TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga DDR3(3/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A228452L-ALG	X01

SHEET 20 of 36



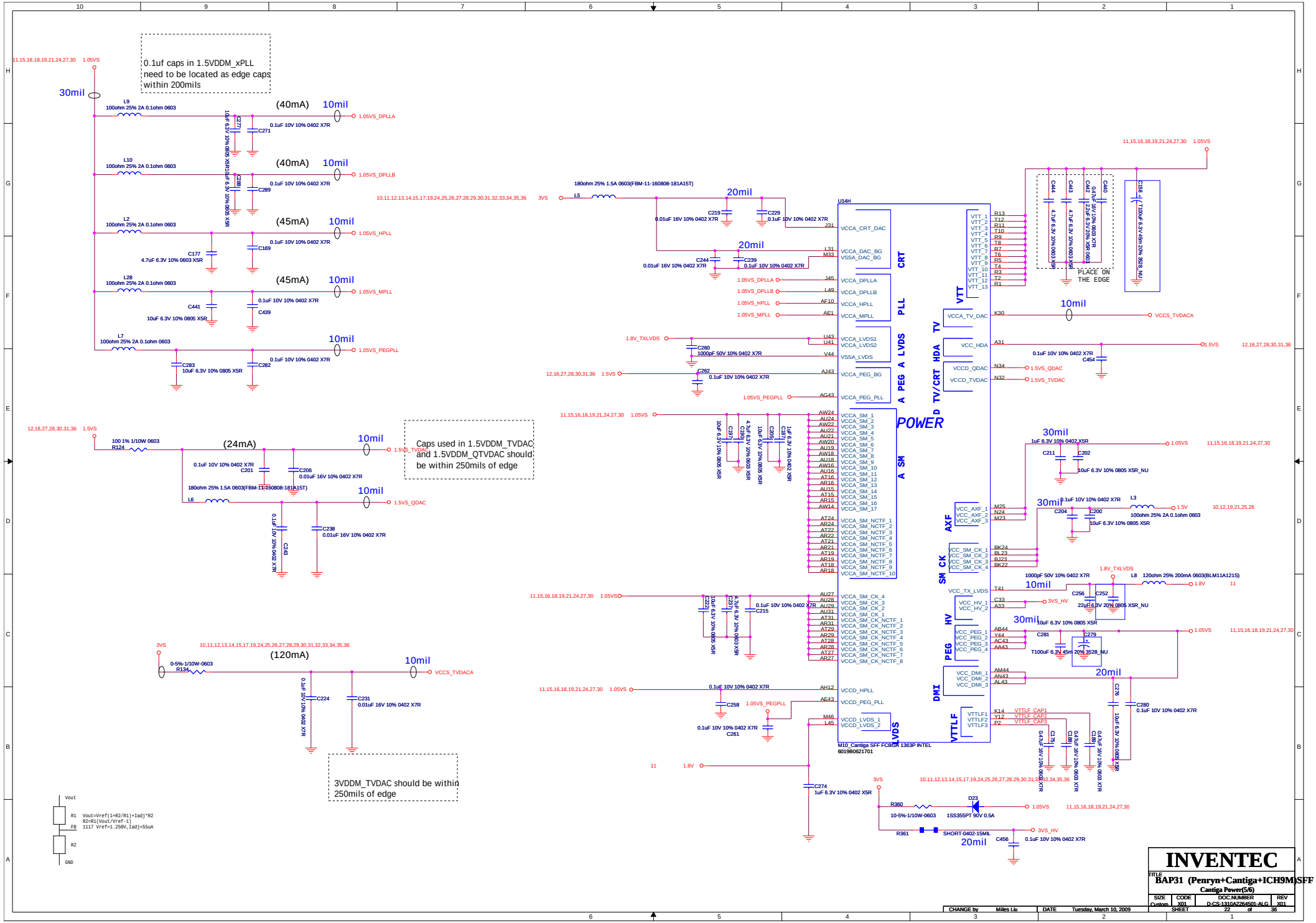
INVENTEC

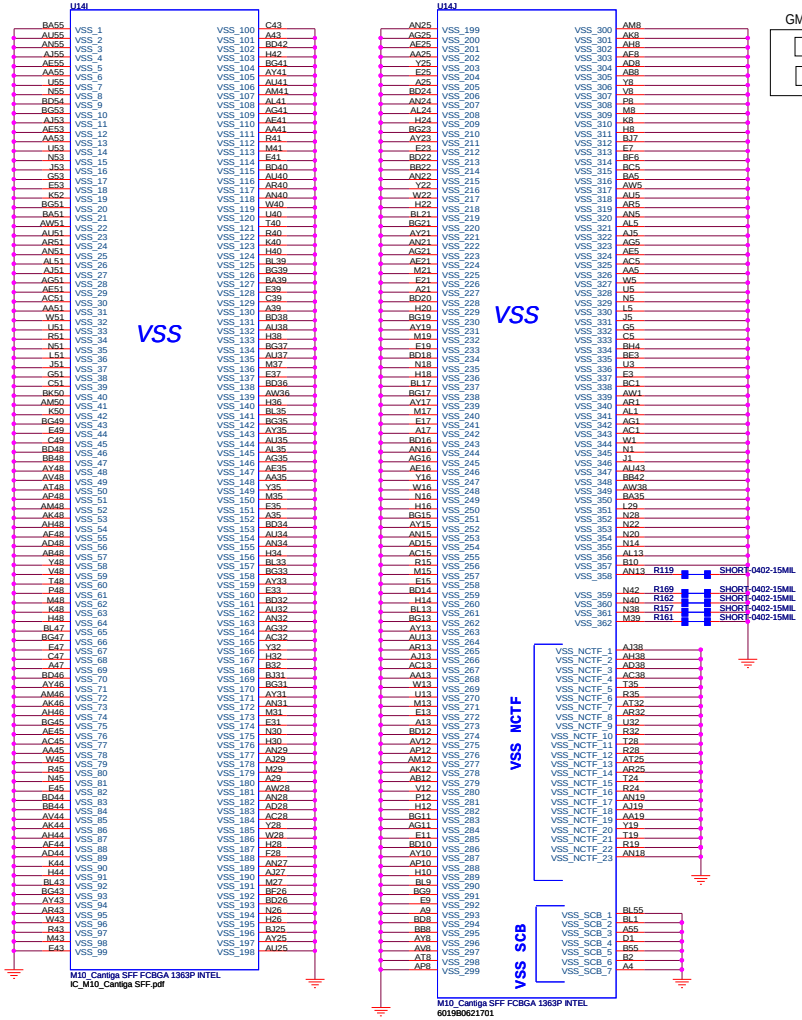
TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Power(4/6)

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A228450L-ALG	X01

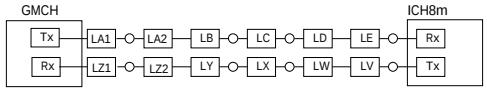
SHEET 21 of 36

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009


0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils
Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge
3VDDM_TVDAC should be within 250mils of edge
PLACE ON THE EDGE
POWER
U14H
M10_Cantiga SFF FCBGA 1363P INTEL
6019B0621701
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Power(5/6)
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A228452L-ALG
REV X01
SHEET 22 of 36
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009



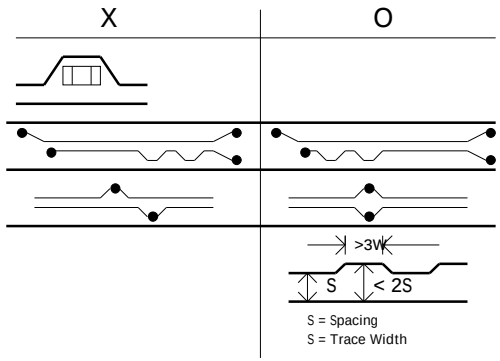
DMI Routing Guideline



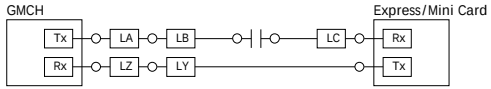
Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



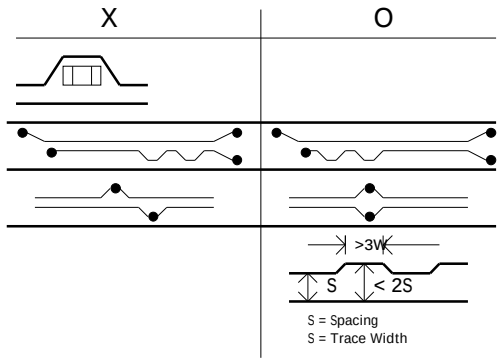
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



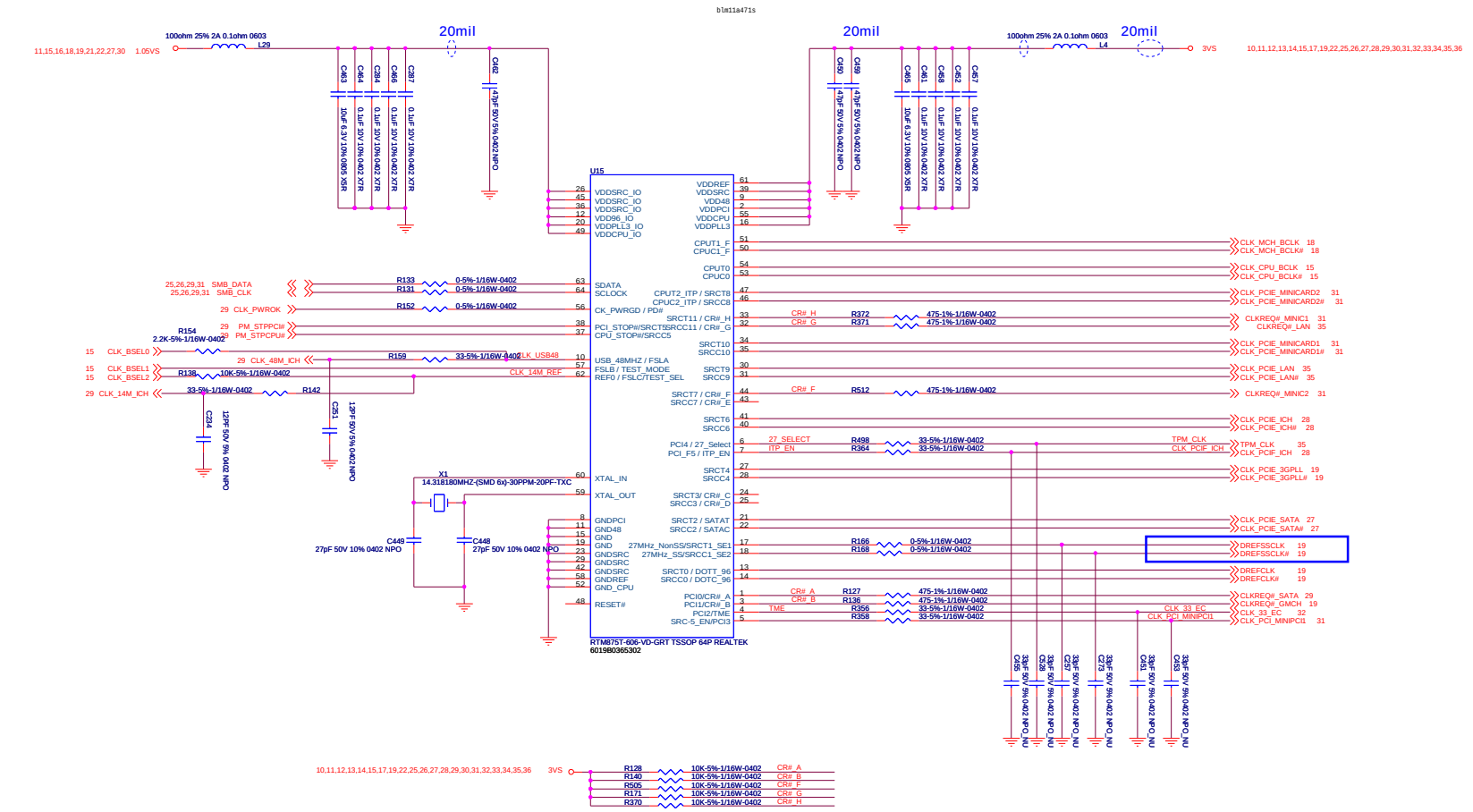
INVENTEC

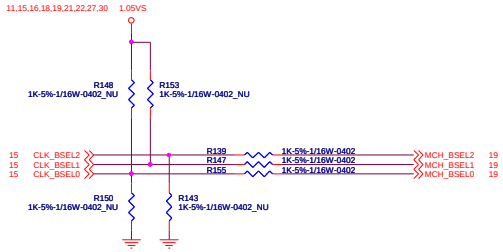
TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
Cantiga Ground(6/6)

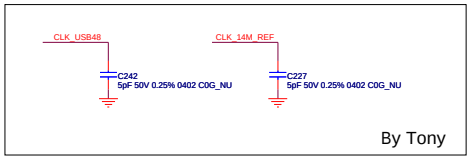
SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET 23 of 36

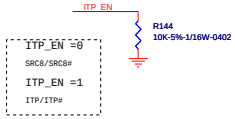
CHANGE by Miles Liu DATE Tuesday, March 10, 2009

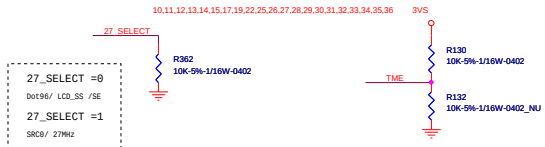






FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY	
1	1	0	667	166	
0	1	0	800	200	
0	0	0	1067	266	*





CR#_A:	Byte 5 bit 6=0--->SRC0 bit 6=1--->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0--->SRC0 bit 2=1--->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0--->SRC1 bit 4=1--->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0--->SRC1 bit 0=1--->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

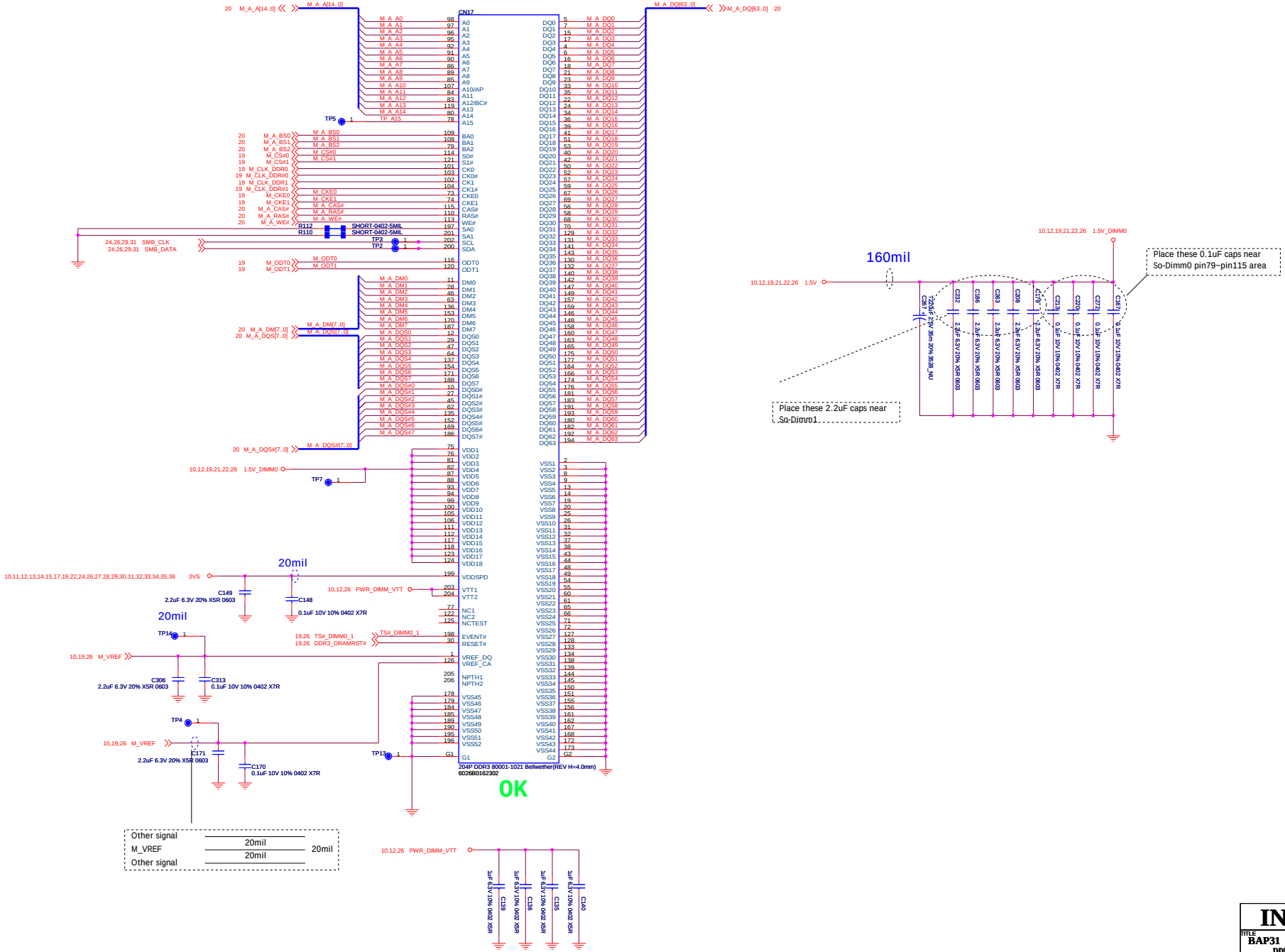
INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
Clock Generator

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009	SHEET	24 of 36

SO-DIMM0



CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009

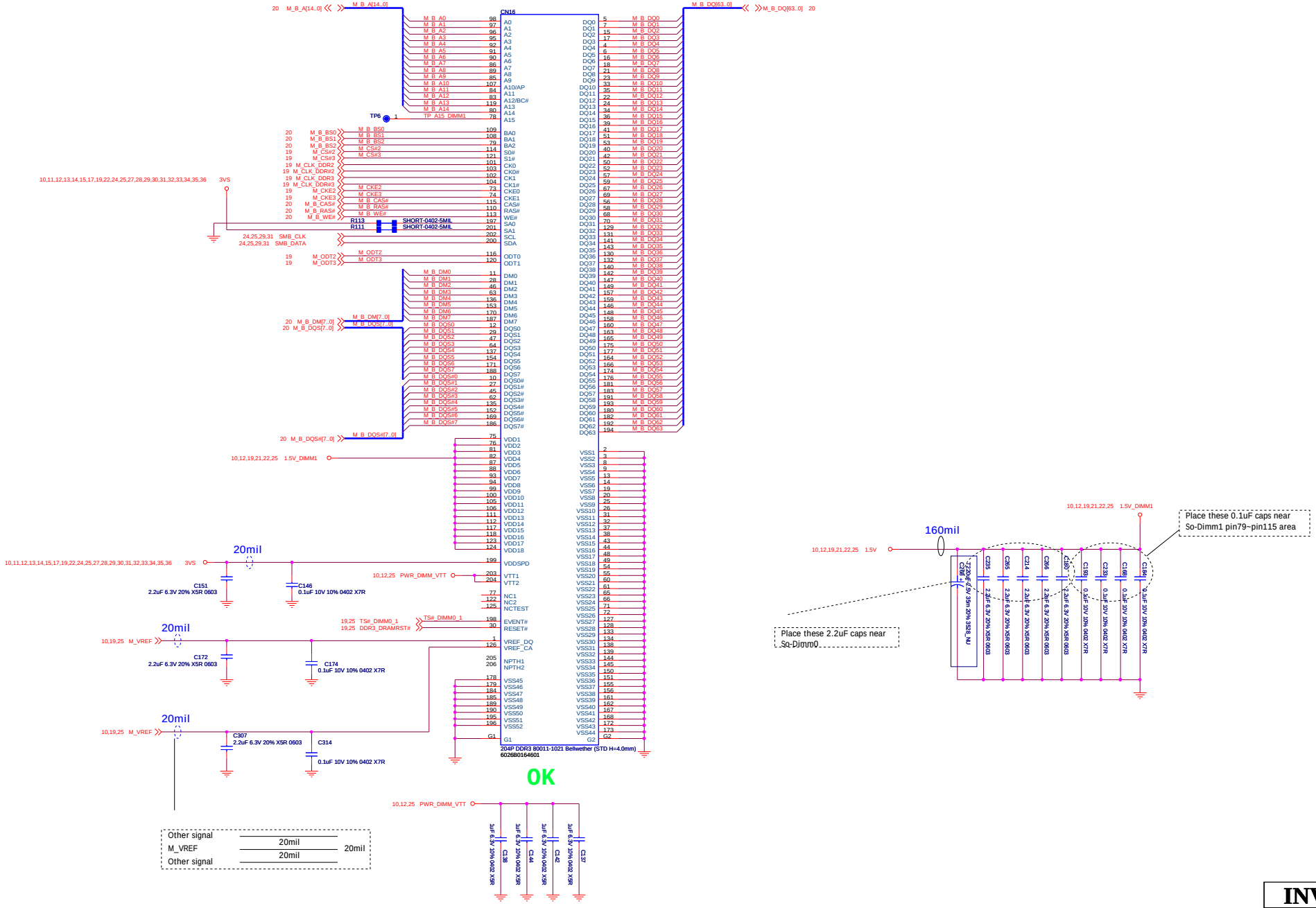
INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF
DDR3 SDRAM SO-DIMM0

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

SHEET

SO-DIMM1

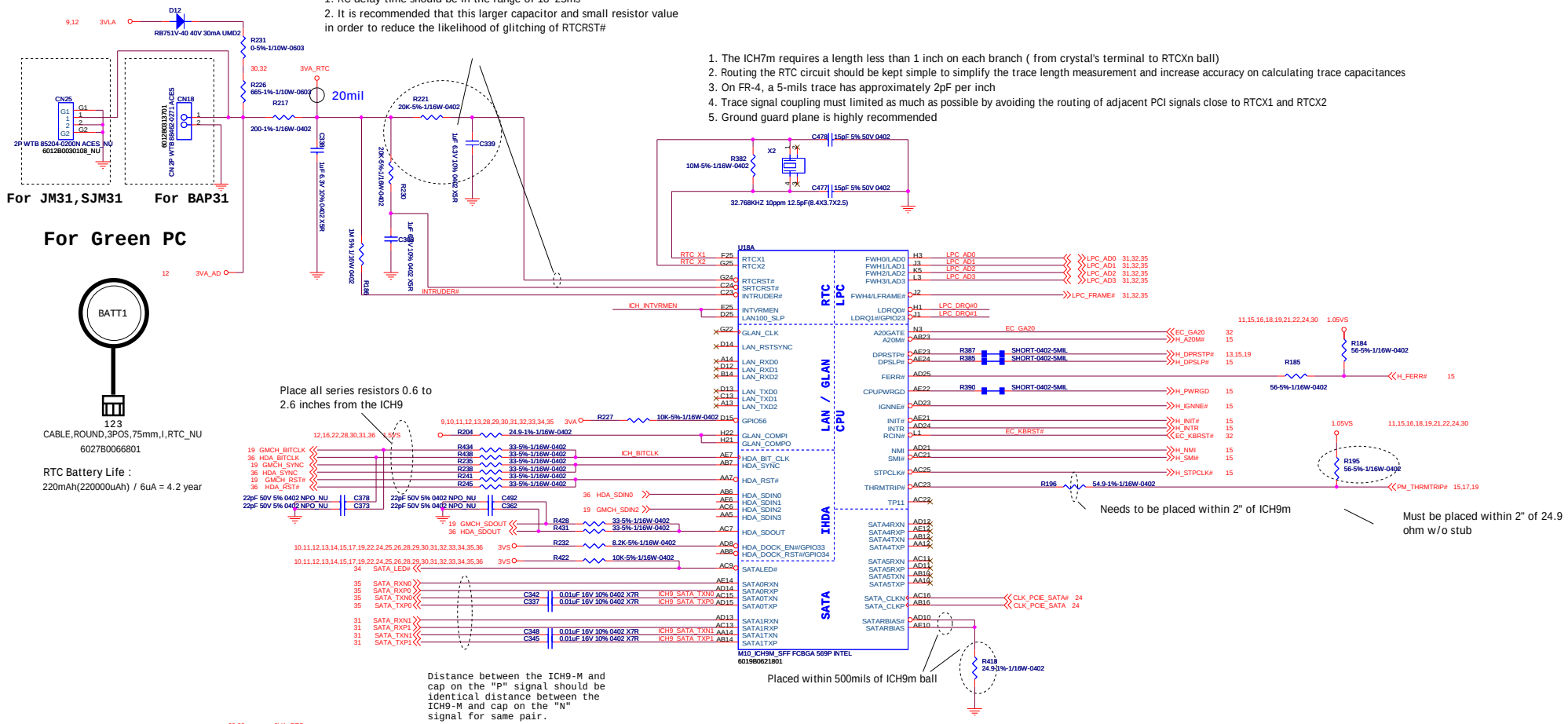


INVENTEC			
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF DDR3 SDRAM SO-DIMM1			
SIZE Custom	CODE X01	DOC.NUMBER D-CS-1310A2264501-ALG	REV X01
CHANGE by Miles Liu	DATE Tuesday, March 10, 2009	SHEET 26 of 36	

RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

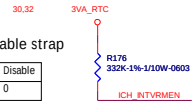
1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended



ICH8m internal VR enable strap

	Enable	Disable
INTVRMEN	1(Default)	0

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05

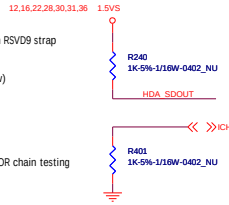


Short pins AG1 and AG2 at the package

ACZ_SDATAOUT strap functionality base on RSVD9 strap

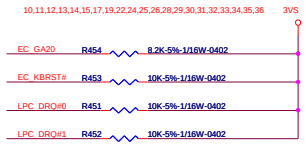
XOR chain entrance (RSVD9 pulled low)

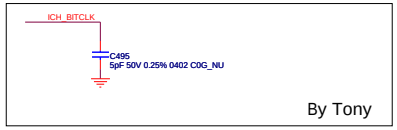
PCIE port config bit 1(RSVD9 not pulled low)



Stuff for XOR chain testing

XOR Chain Entrance Strap - to be updated		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

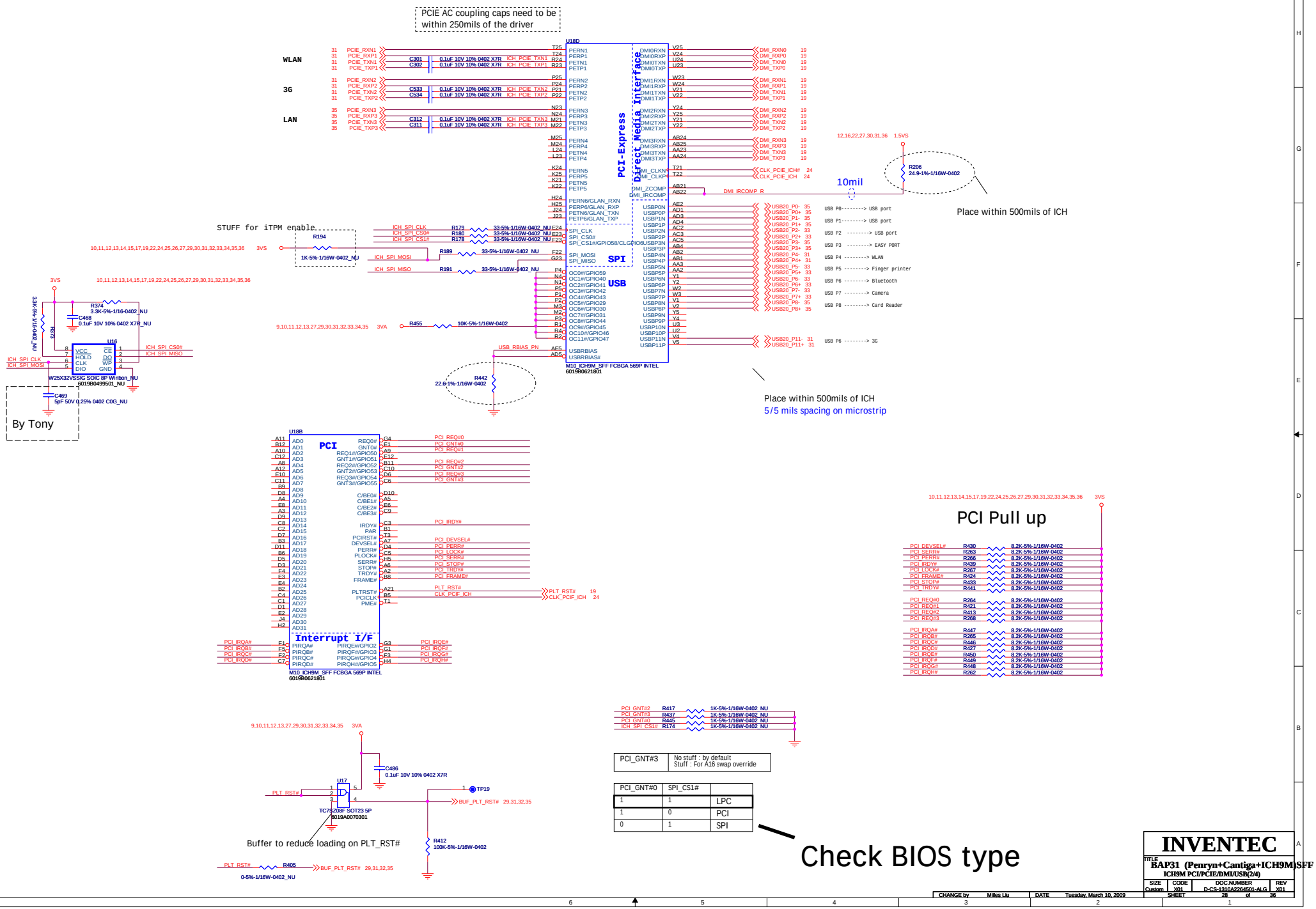




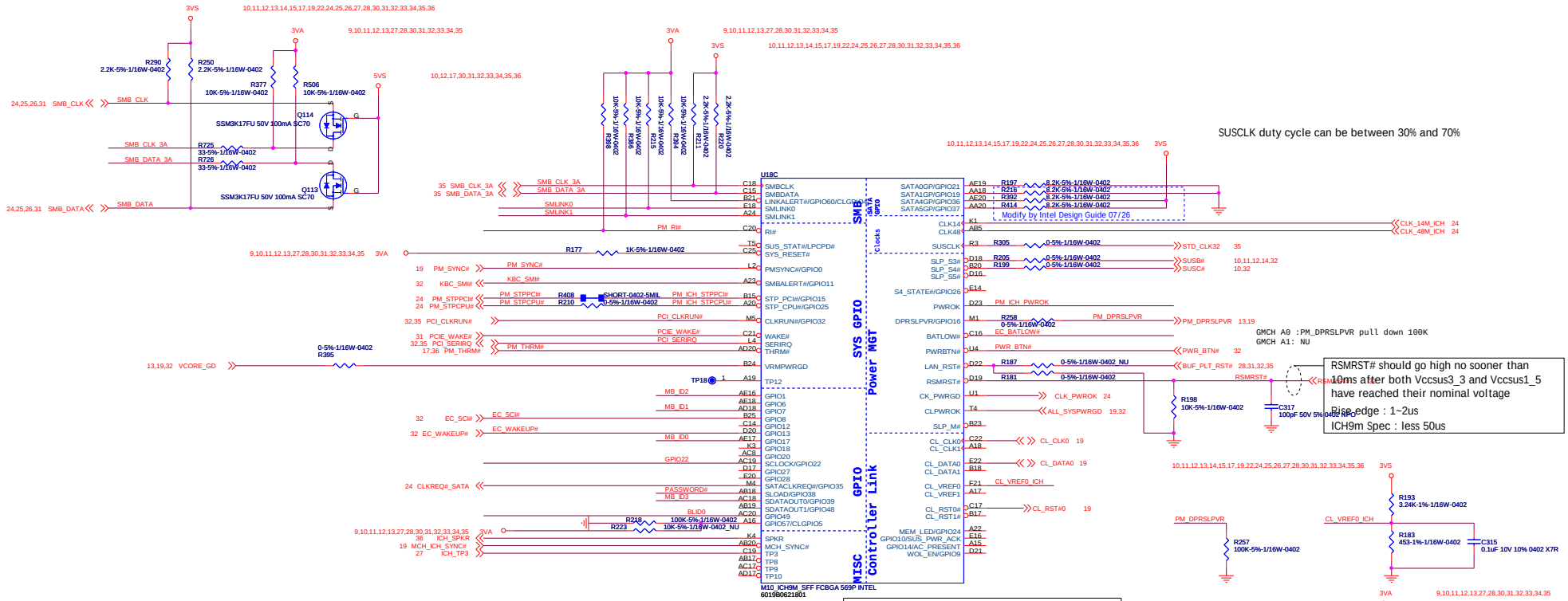
By Tony

INVENTEC			
TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF ICH9M CPU/IDE/SATA(1/4)			
SIZE: Custom	CODE: X01	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: X01
SHEET			

CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009



PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI



BIOS ID setting

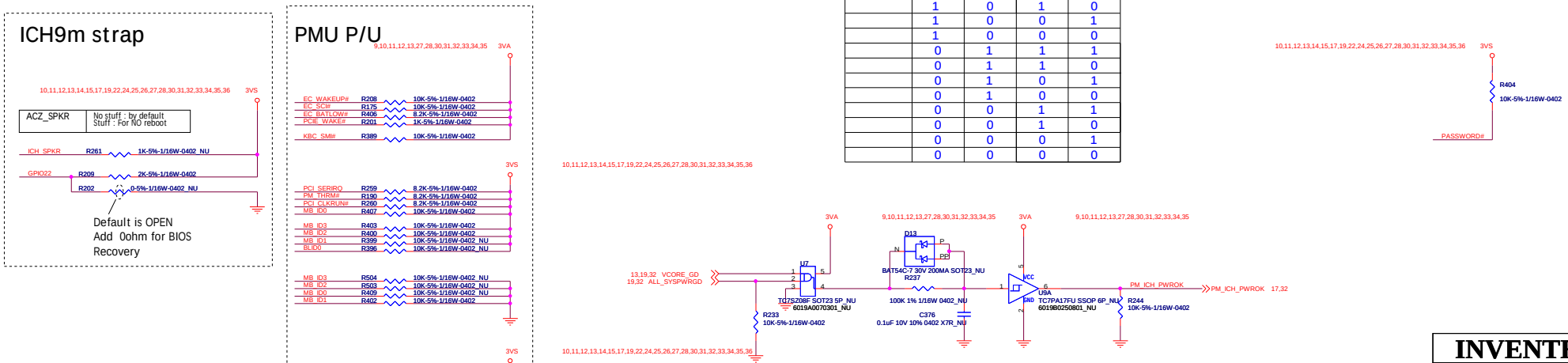
Project	MB_ID3	MB_ID2	MB_ID1	MB_ID0
JM31 (UMA)	1	1	1	1
SJM31 (UMA)	1	1	1	0
BAP31 (UMA)	1	1	0	1
	1	1	0	0
	1	0	1	1
	1	0	1	0
	1	0	0	1
	1	0	0	0
	0	1	1	1
	0	1	1	0
	0	1	0	1
	0	1	0	0
	0	0	1	1
	0	0	1	0
	0	0	0	1
	0	0	0	0

ICH9m strap

ACZ_SPKR	No stuff : by default Stuff : For NO reboot

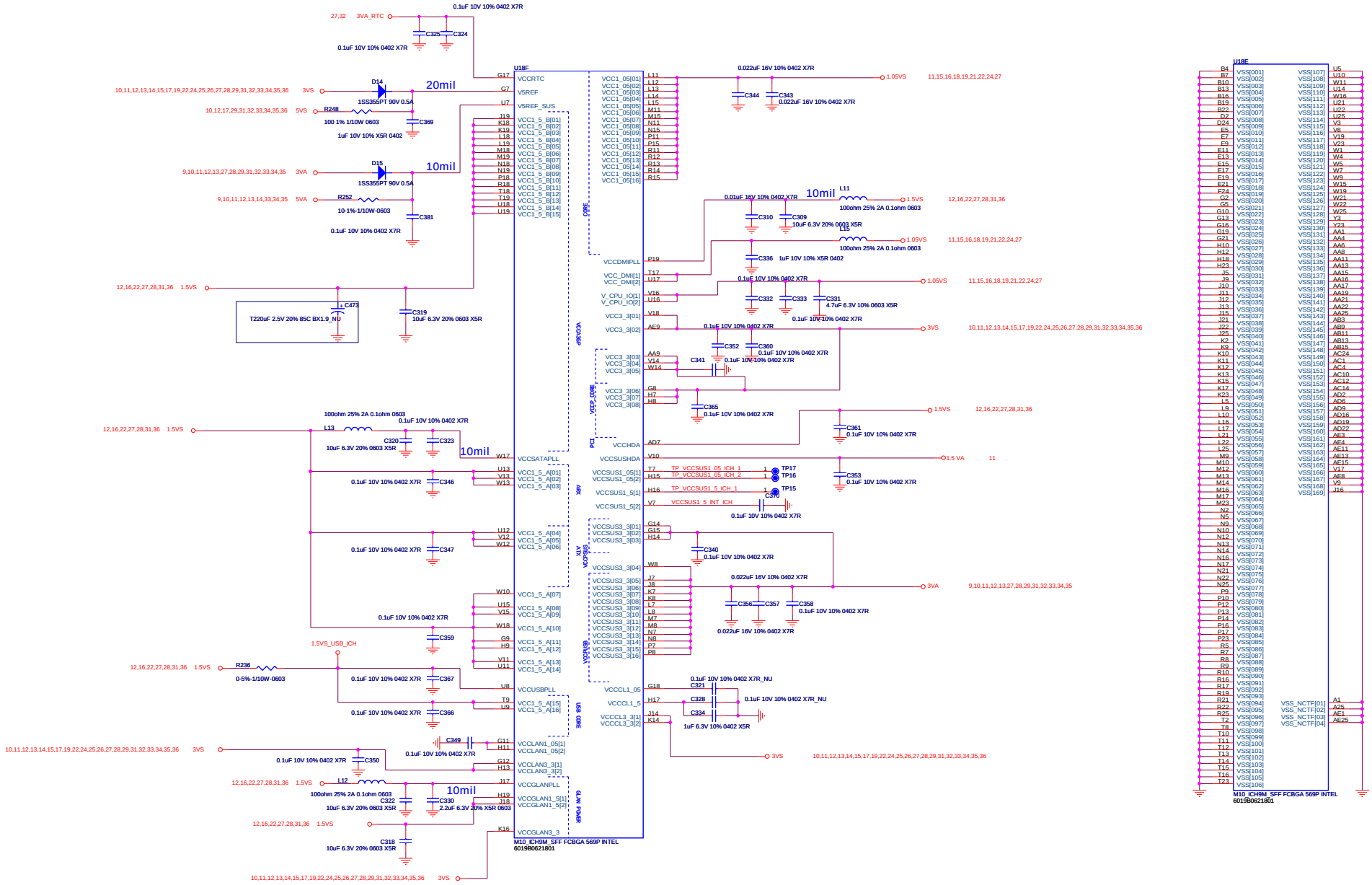
Default is OPEN
Add 0ohm for BIOS Recovery

PMU P/U



INVENTEC			
TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF ICH9M GPIO(3/4)			
SIZE: Custom	CODE: X01	DOC.NUMBER: D-CS-1310A2264501-ALG	REV: X01
SHEET			

CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009

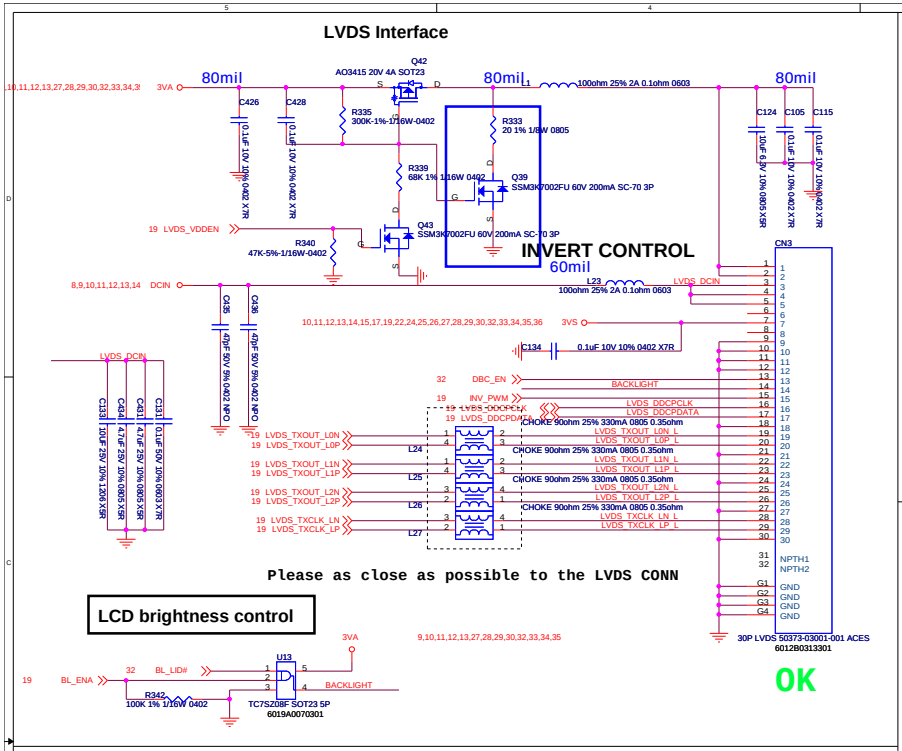


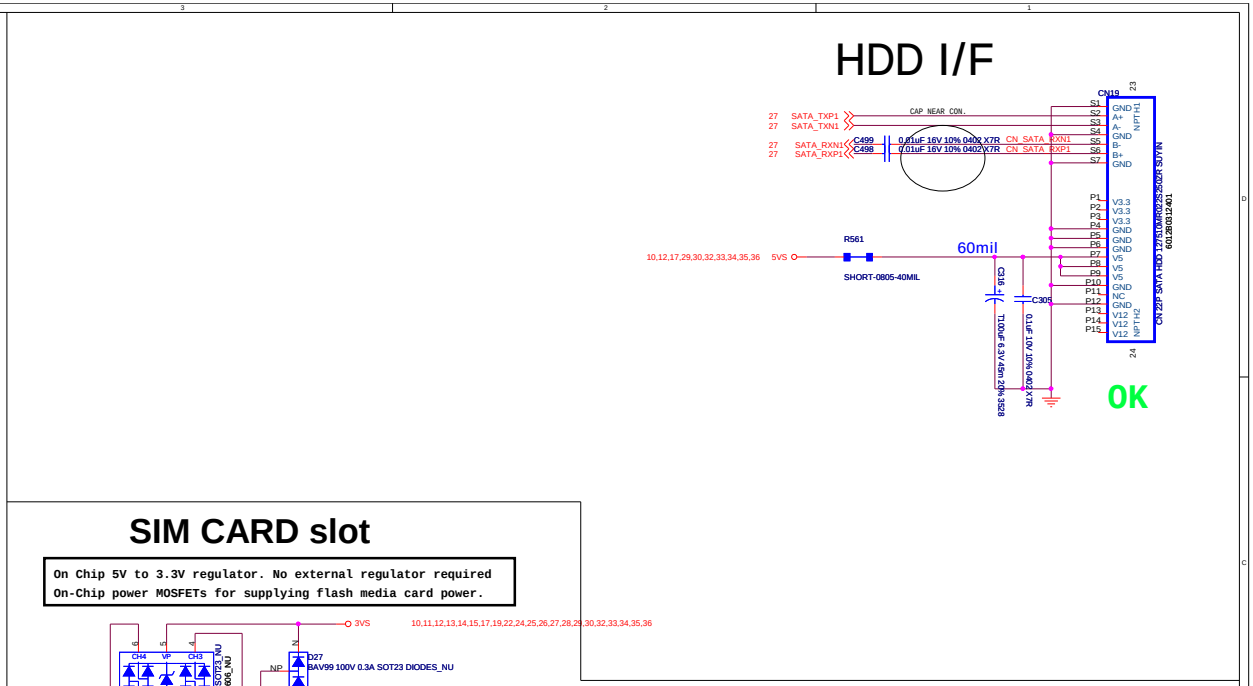
INVENTEC

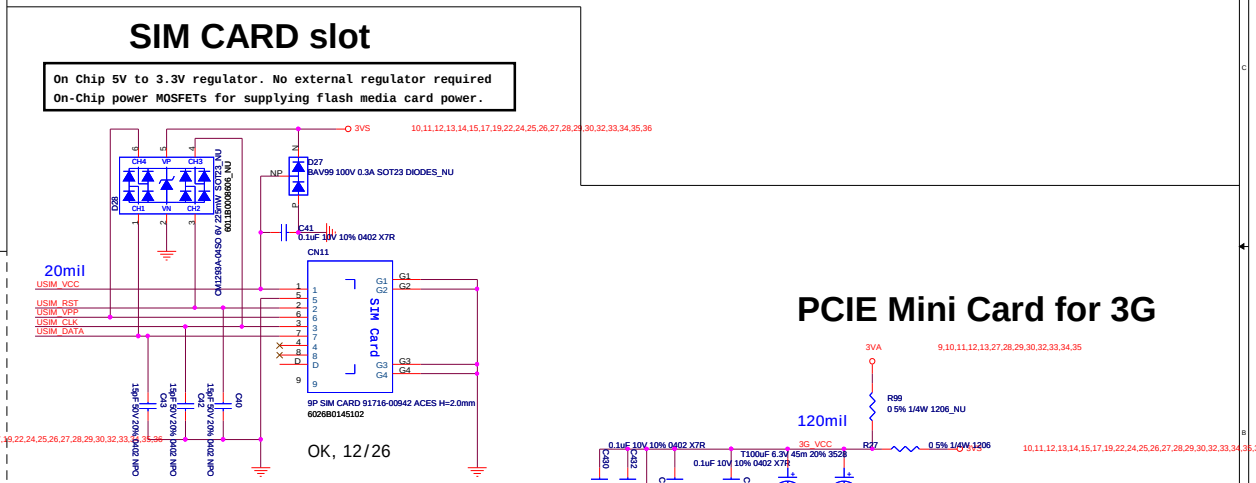
TITLE
BAP31 (Penryn+Cantiga+ICH9M)SFF
ICH9M Power/GND(4/4)

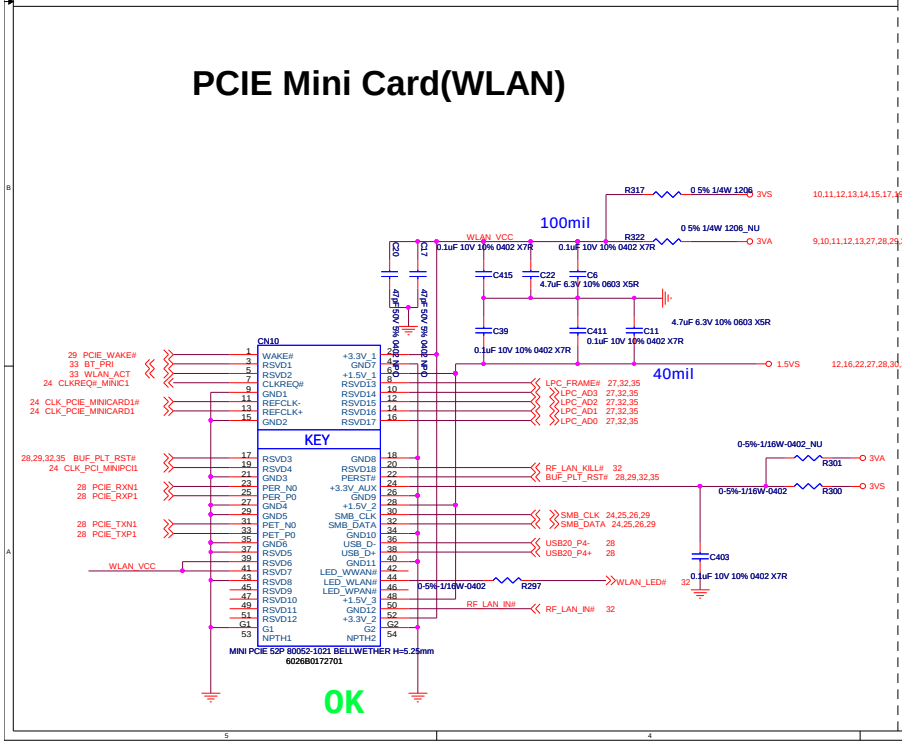
SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

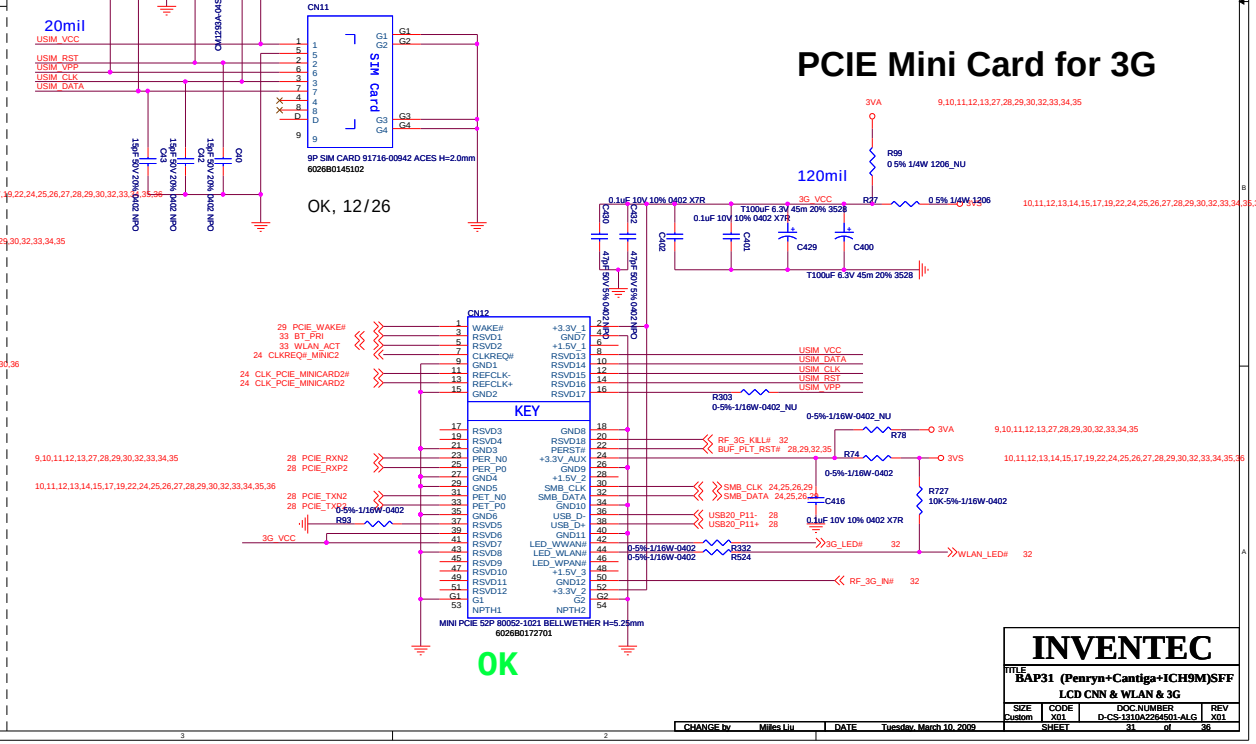
CHANGE by: Miles Liu | DATE: Tuesday, March 10, 2009 | SHEET 30 of 36









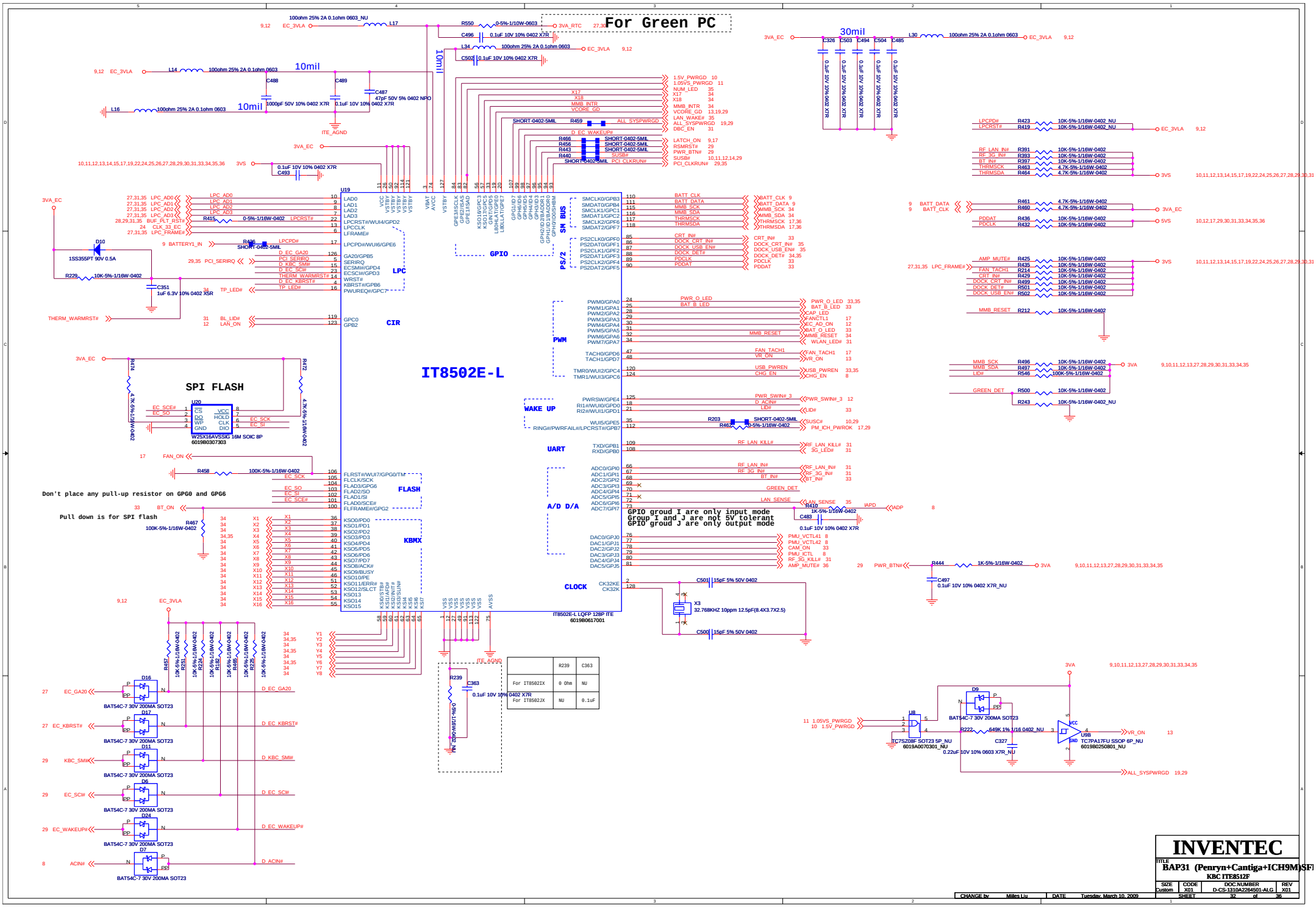


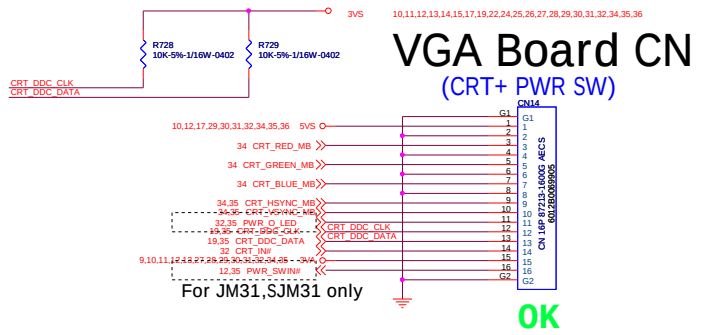
INVENTEC

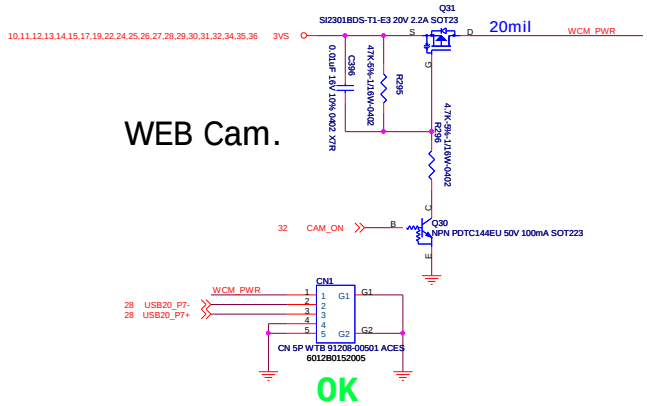
TITLE BAP31 (Penryn+Cantiga+ICH9M)SFF
LCD CNN & WLAN & 3G

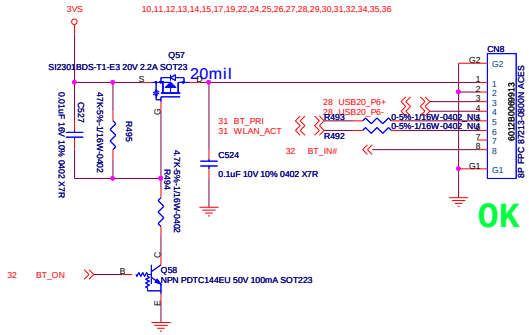
SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

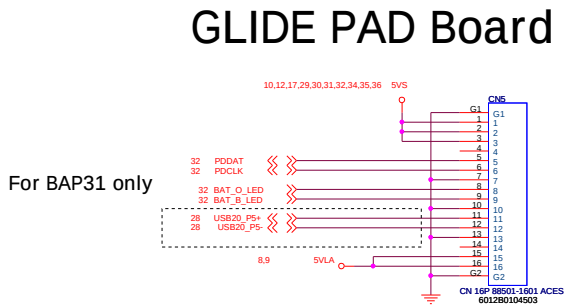
CHANGE by Miles Liu DATE Tuesday, March 10, 2009 SHEET 31 of 36

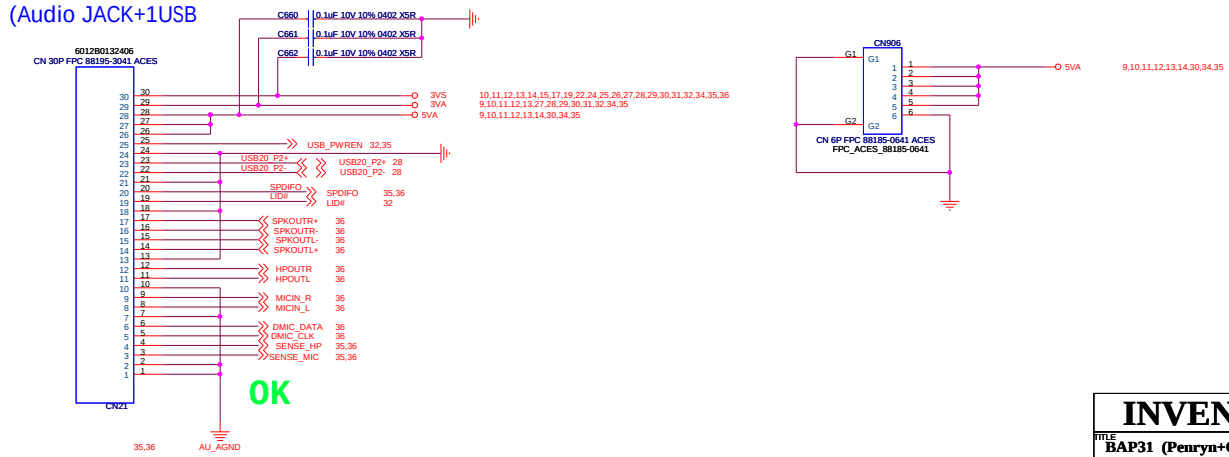

For Green PC
IT8502E-L
SPI FLASH
W25X16AVSSIG 16M SOIC 8P
6019B0307303
IT8502E-L LQFP 128P ITE
6019B0617001
Don't place any pull-up resistor on GPG0 and GPG6
Pull down is for SPI flash
GPIO groud I are only input mode
Group I and J are not 5V tolerant
GPIO groud J are only output mode
LPC
CIR
FLASH
KBMX
GPIO
SM BUS
PS/2
PWM
WAKE UP
UART
A/D D/A
CLOCK
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
KBC ITE8512F
DOC.NUMBER D-CS-1310A2264501-ALG
SHEET 32 of 36
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009











INVENTEC

TITLE BAP31 (Penryn+Cantiga+ICH9M)SI
Daughter Connector

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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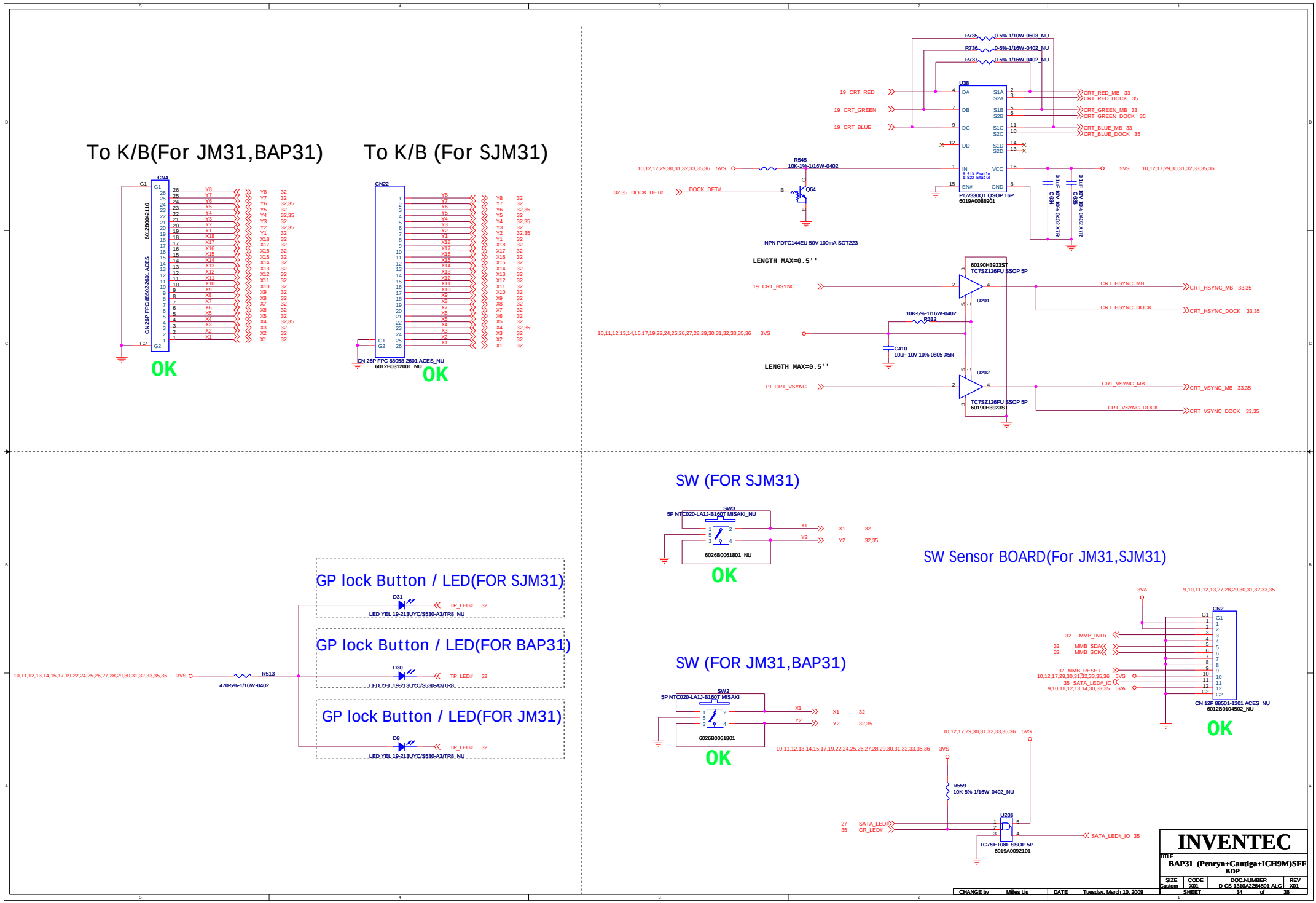
CHANGE by Miles Liu DATE Tuesday, March 10, 2009


To K/B(For JM31,BAP31)
To K/B (For SJM31)
CN4
CN 26P FPC 88502-2601 ACES
6012B0042110
OK
CN22
CN 26P FPC 88058-2601 ACES_NU
6012B0312001_NU
OK
R735 0-5%-1/10W-0603_NU
R736 0-5%-1/16W-0402_NU
R737 0-5%-1/16W-0402_NU
U38
PI5V330Q1 QSOP 16P
6019A0088901
R545 10K-1%-1/16W-0402
Q64
NPN PDTC144EU 50V 100mA SOT223
C434 0.1uF 10V 10% 0402 X7R
C435 0.1uF 10V 10% 0402 X7R
LENGTH MAX=0.5''
60190H3923ST
TC7SZ126FU SSOP 5P
U201
U202
R312 10K-5%-1/16W-0402
C410 10uF 10V 10% 0805 X5R
CRT_HSYNC_MB
CRT_HSYNC_DOCK
CRT_VSYNC_MB
CRT_VSYNC_DOCK
SW (FOR SJM31)
SW3
5P NTC020-LA1J-B160T MISAKI_NU
6026B0061801_NU
OK
SW Sensor BOARD(For JM31,SJM31)
CN2
CN 12P 88501-1201 ACES_NU
6012B0104502_NU
OK
GP lock Button / LED(FOR SJM31)
D31
LED YEL 19-213/UYC/S530-A3/TR8_NU
GP lock Button / LED(FOR BAP31)
D30
LED YEL 19-213/UYC/S530-A3/TR8
GP lock Button / LED(FOR JM31)
D8
LED YEL 19-213/UYC/S530-A3/TR8_NU
R513 470-5%-1/16W-0402
SW (FOR JM31,BAP31)
SW2
5P NTC020-LA1J-B160T MISAKI
6026B0061801
OK
R559 10K-5%-1/16W-0402_NU
U203
TC7SET08F SSOP 5P
6019A0092101
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF BDP
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
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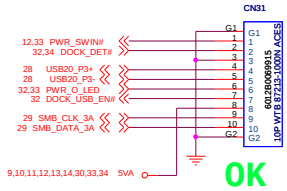
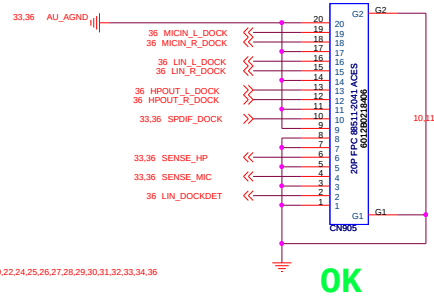
CHANGE by Miles Liu
DATE Tuesday, March 10, 2009

For BAP31(EASY/B)

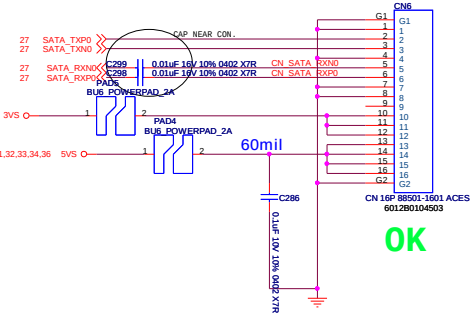
MB(USB) TO EASY/B



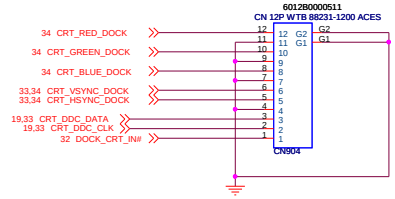
MB(AUDIO) TO EASY/B(For BAP31)



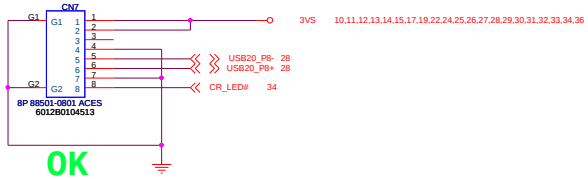
SSD I/F



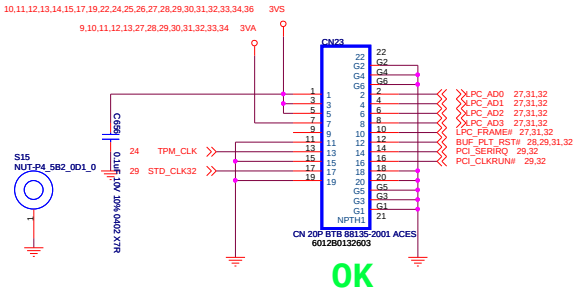
MB(RGB) TO EASY/B



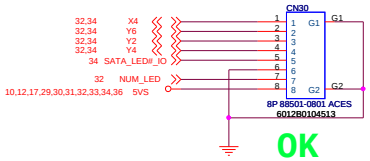
Card Reader BOARD CN

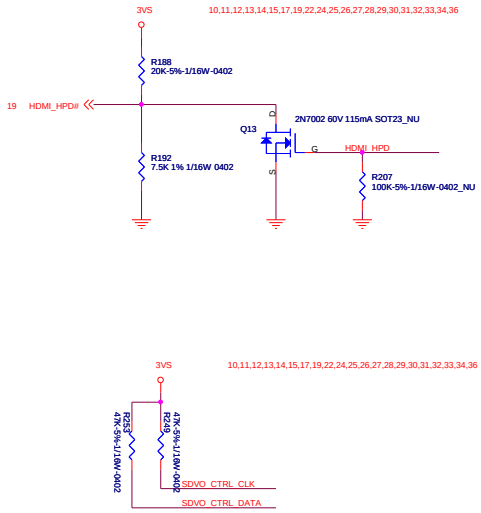


TPM CN

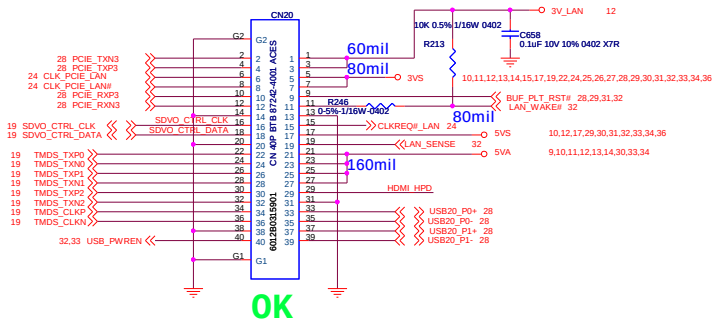


SW/B CN





USB Board CN
(LAN+HDMI+2USB)



CHANGE by	Miles Liu	DATE	Tuesday, March 10, 2009		

INVENTEC

TITLE: BAP31 (Penryn+Cantiga+ICH9M)SFF BDP

SIZE	CODE	DOC.NUMBER	REV
Custom	X01	D-CS-1310A2264501-ALG	X01

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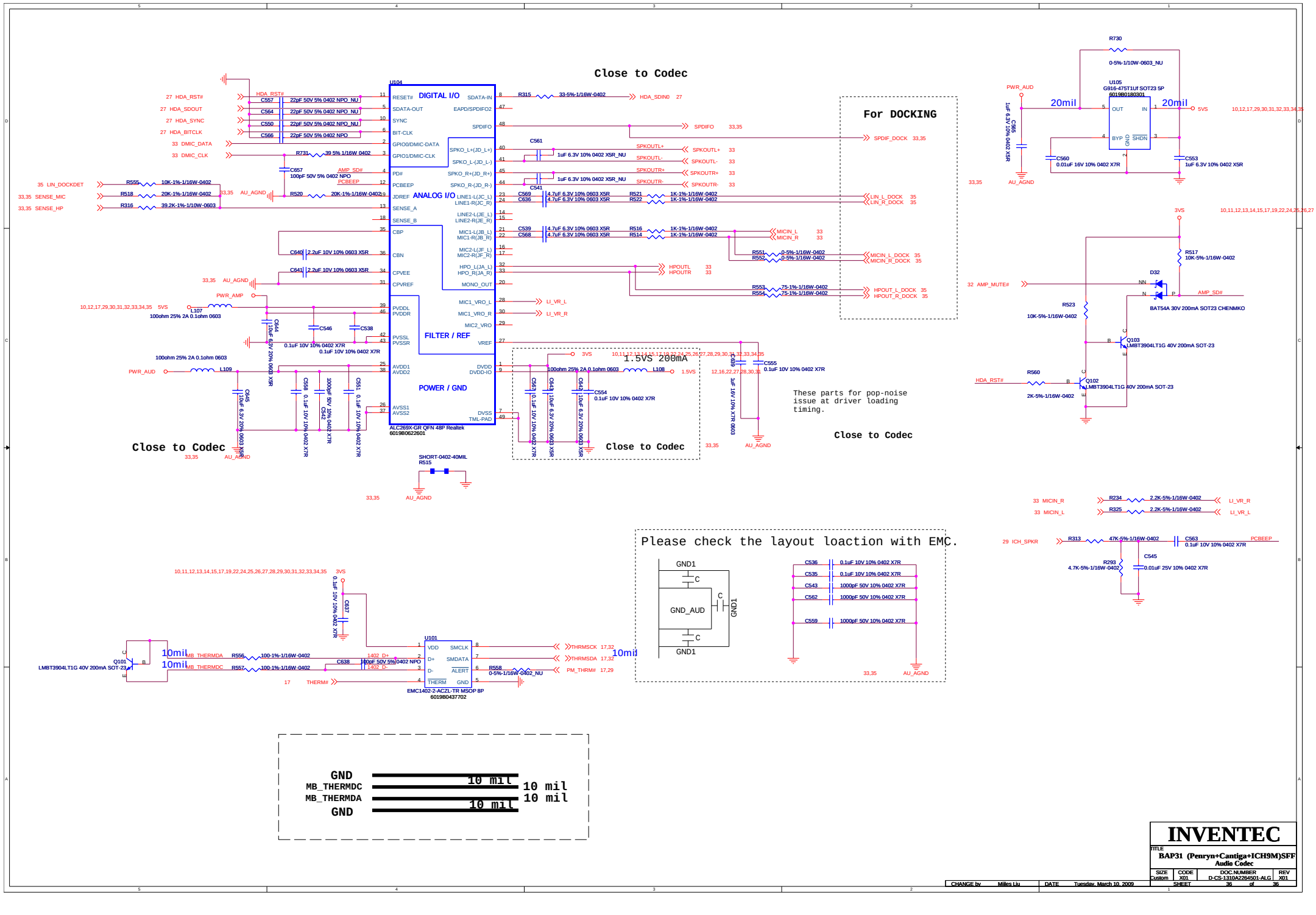
Close to Codec
U104
DIGITAL I/O
ANALOG I/O
FILTER / REF
POWER / GND
ALC269X-GR QFN 48P Realtek
6019B0622601
For DOCKING
U105
G916-475T1U/f SOT23 5P
6019B0180301
20mil
20mil
1.5VS 200mA
These parts for pop-noise issue at driver loading timing.
Close to Codec
Close to Codec
Close to Codec
SHORT-0402-40MIL
R515
U101
EMC1402-2-ACZL-TR MSOP 8P
6019B0437702
LMBT3904LT1G 40V 200mA SOT-23
Please check the layout loaction with EMC.
GND1
GND_AUD
GND1
GND1
GND
MB_THERMDC
MB_THERMDA
GND
10 mil
10 mil
10 mil
10 mil
INVENTEC
BAP31 (Penryn+Cantiga+ICH9M)SFF
Audio Codec
SIZE Custom
CODE X01
DOC.NUMBER D-CS-1310A2264501-ALG
REV X01
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CHANGE by Miles Liu
DATE Tuesday, March 10, 2009